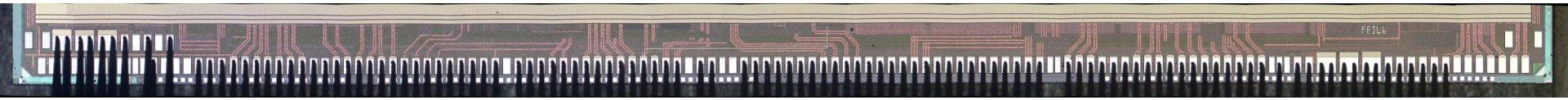
universitätbonn

# FE-I4B wafer probing



ATLAS IBL General Meeting
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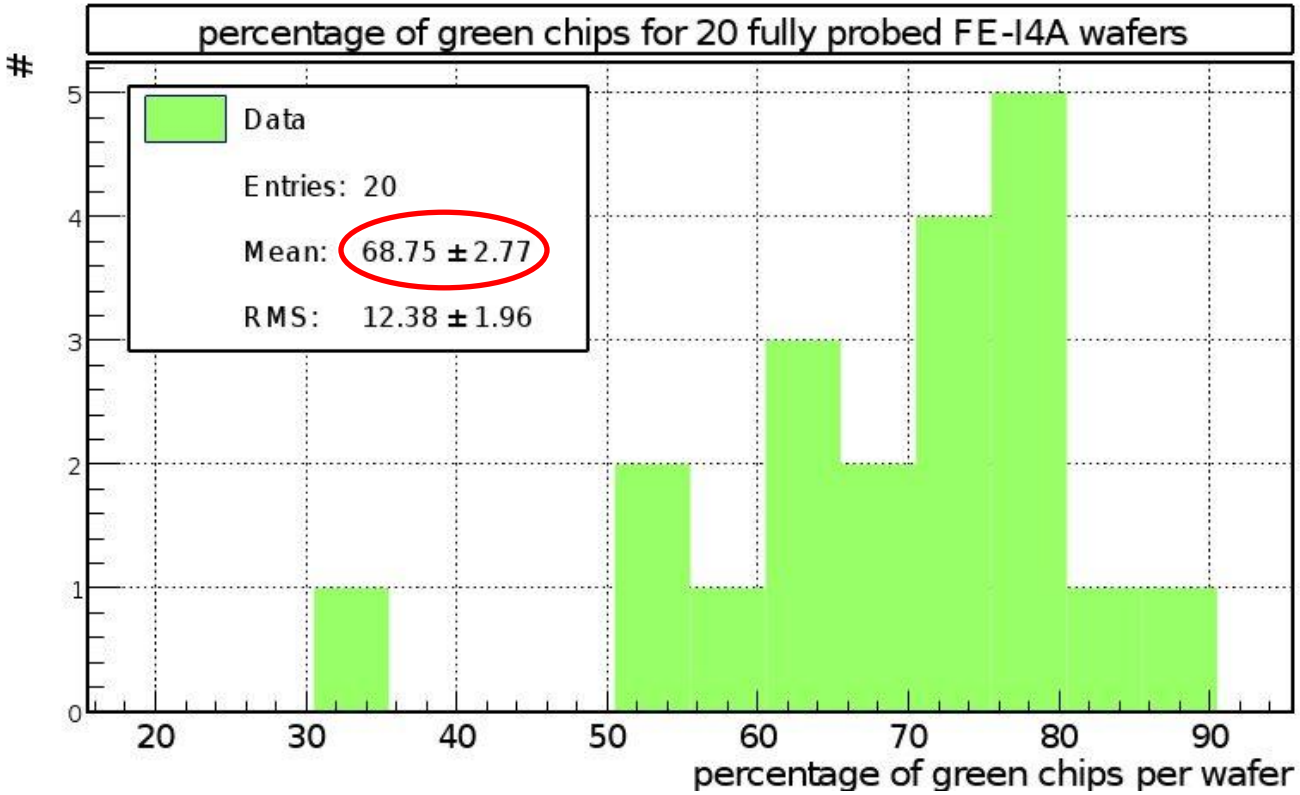
# FE-I4A wafer probing summary

- 20 FE-I4A wafers fully probed (80% Bonn, 20% Berkeley)
- 2 unprobed wafers for diced chips
- 4 at Aptasic
- 14 unprobed FE-I4A  wafers in Bonn
- Time needed per wafer for one run: 35 h
- Yield of green chips: (69 ± 3)%



# From FE-I4A to FE-I4B wafer probing I

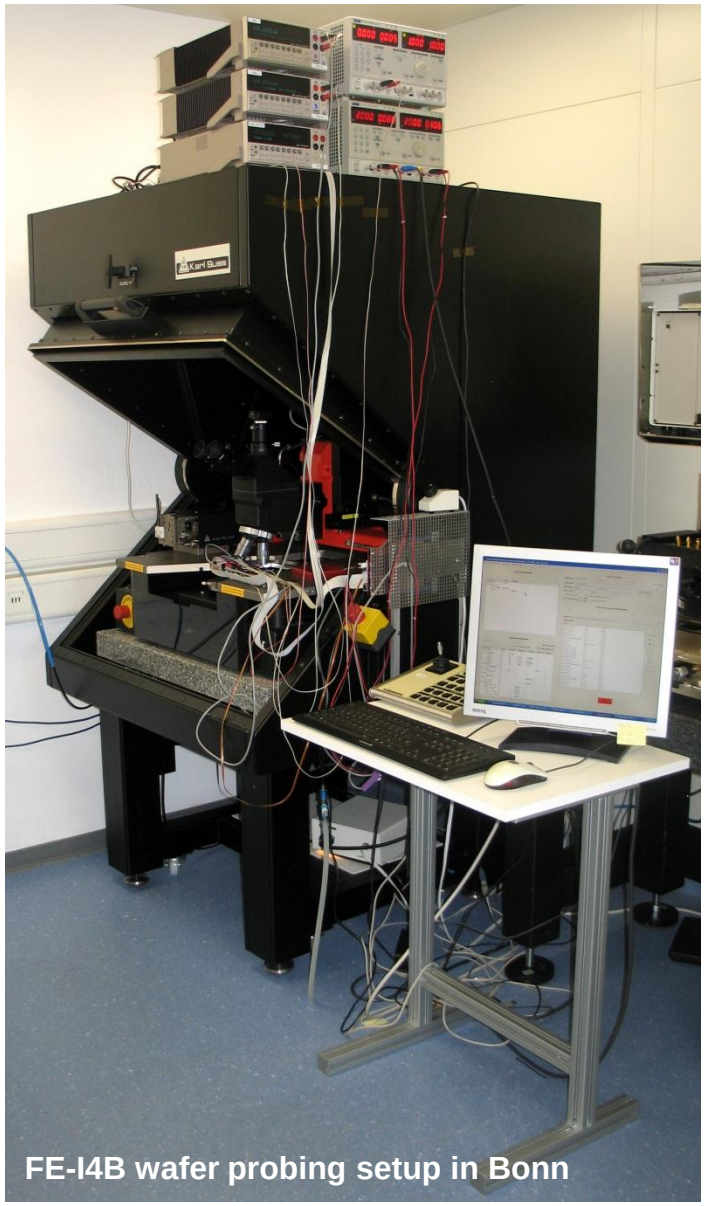
Many new things to do at wafer level (written in red)

- Chip testing:
  - Current consumption after power up and after configuration
  - Scan chain tests for 3 peripheral digital logic blocks (DOB, CMD, ECL)
  - Analog/digital scan
  - Latency counter test (in each PDR)
  - Global and pixel register tests
  - Analog/digital band gap references, analog/digital Vrefs from Iref
  - Buffer ToT test (for each pixel)
  - Hit Or test
  - threshold scan
  - analog/digital scan
  - Clow/Chigh analog scan
  - Crosstalk scan
  - Current @ high trigger frequency test
  - Injection delay scan
  - Service records
- Chip calibration on wafer level:
  - Reference current tuning
  - Pulser DAC transfer function
  - Injection capacitance measurement
  - Measurement of the digital/analog band gap and digital/analog voltage references
  - 15-bit serial number burning: chip number (6-bit), wafer number (9-bit)

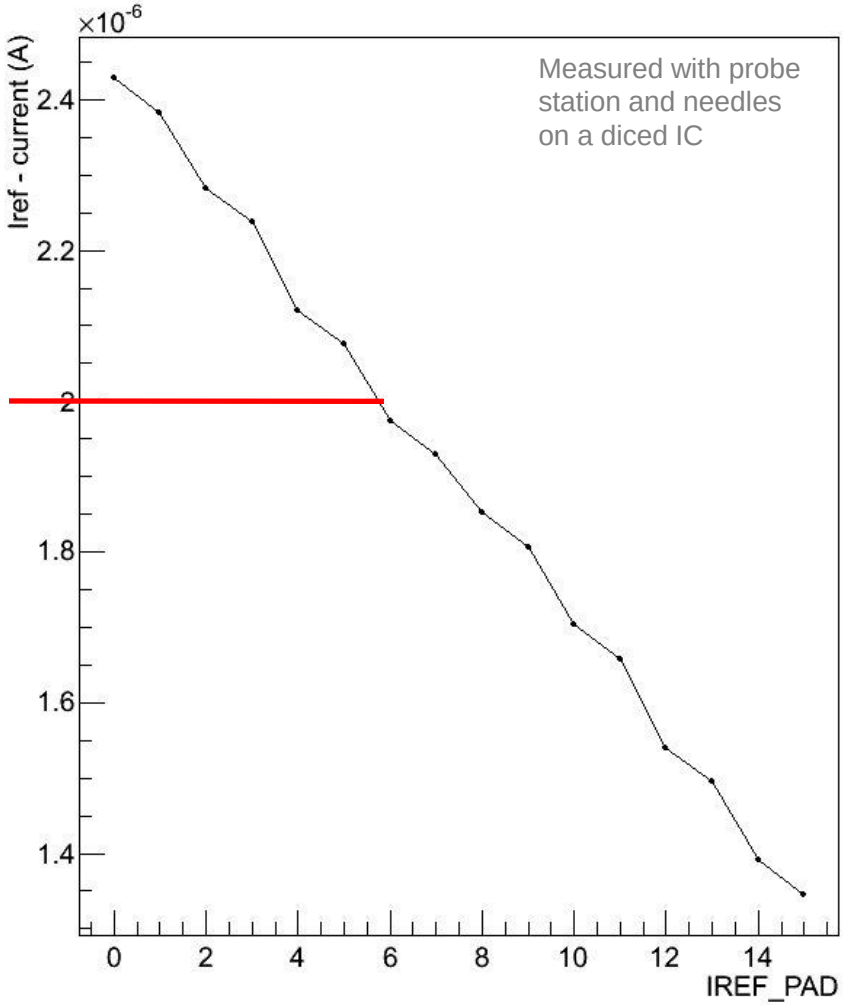
# From FE-I4A to FE-I4B wafer probing II

- Hardware:
  - FE-I4B requires new PCB with new needle card
  - Extended hardware setup to:
    - Tune the reference current ⇦
    - Measure the PlsrDAC transfer function
    - Measure the digital/analog band gap references
    - Measure the tunable analog/digital references
    - Measure Injection capacitance ⇦
    - Trigger the chip serial number burning

⇦ Shown on following slides

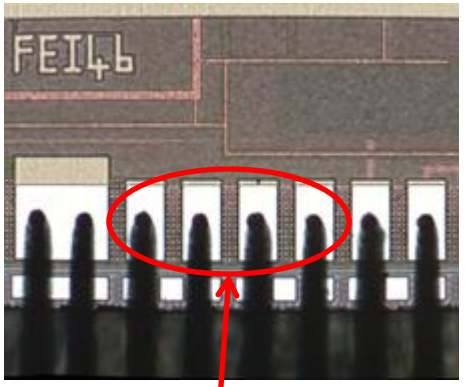

FE-I4B wafer probing setup in Bonn

# Current reference (Iref) tuning



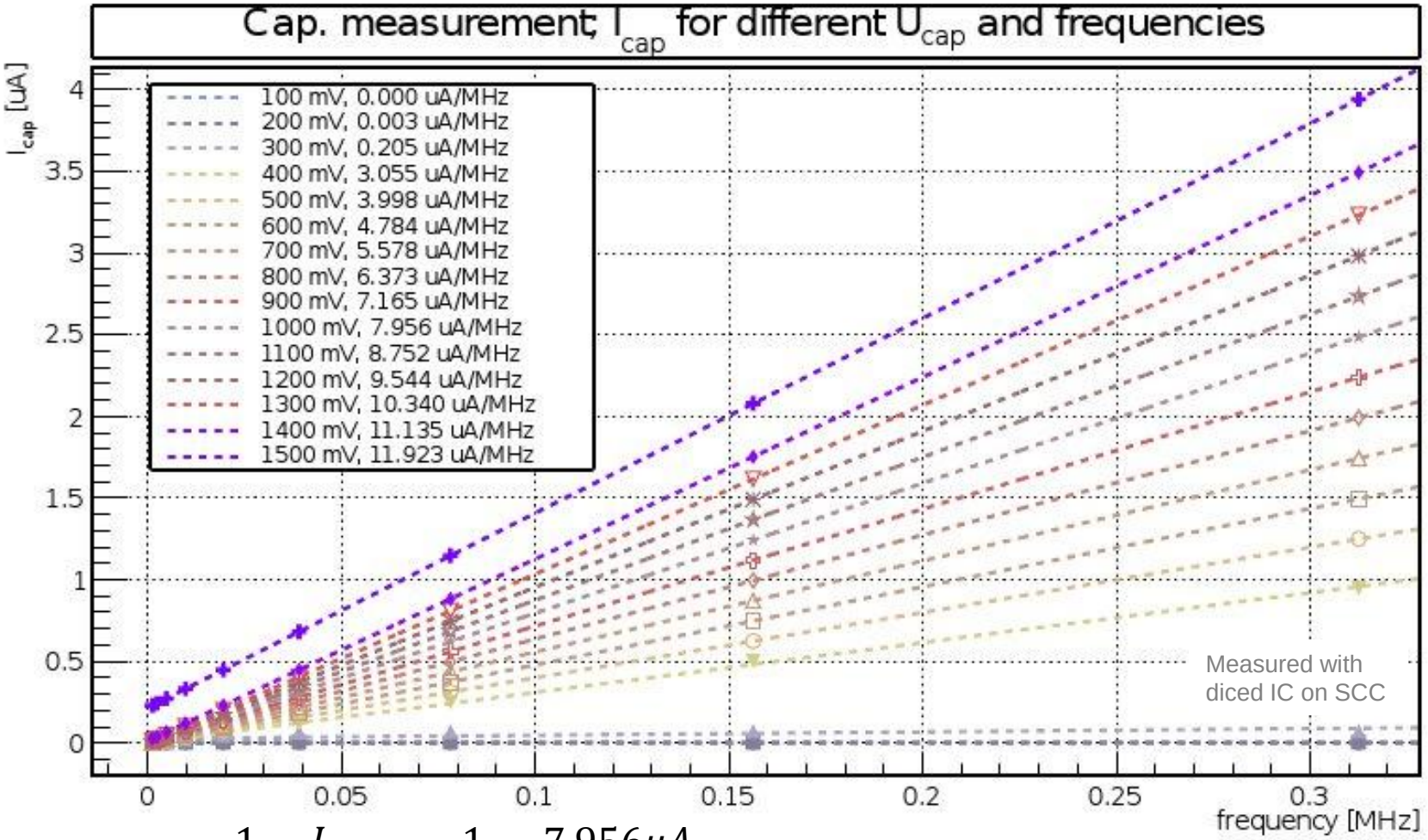

tune to 2 uA

MSB LSB




- In FE-I4B: reference current can only be changed by Iref Pads
  → no access with the module flex

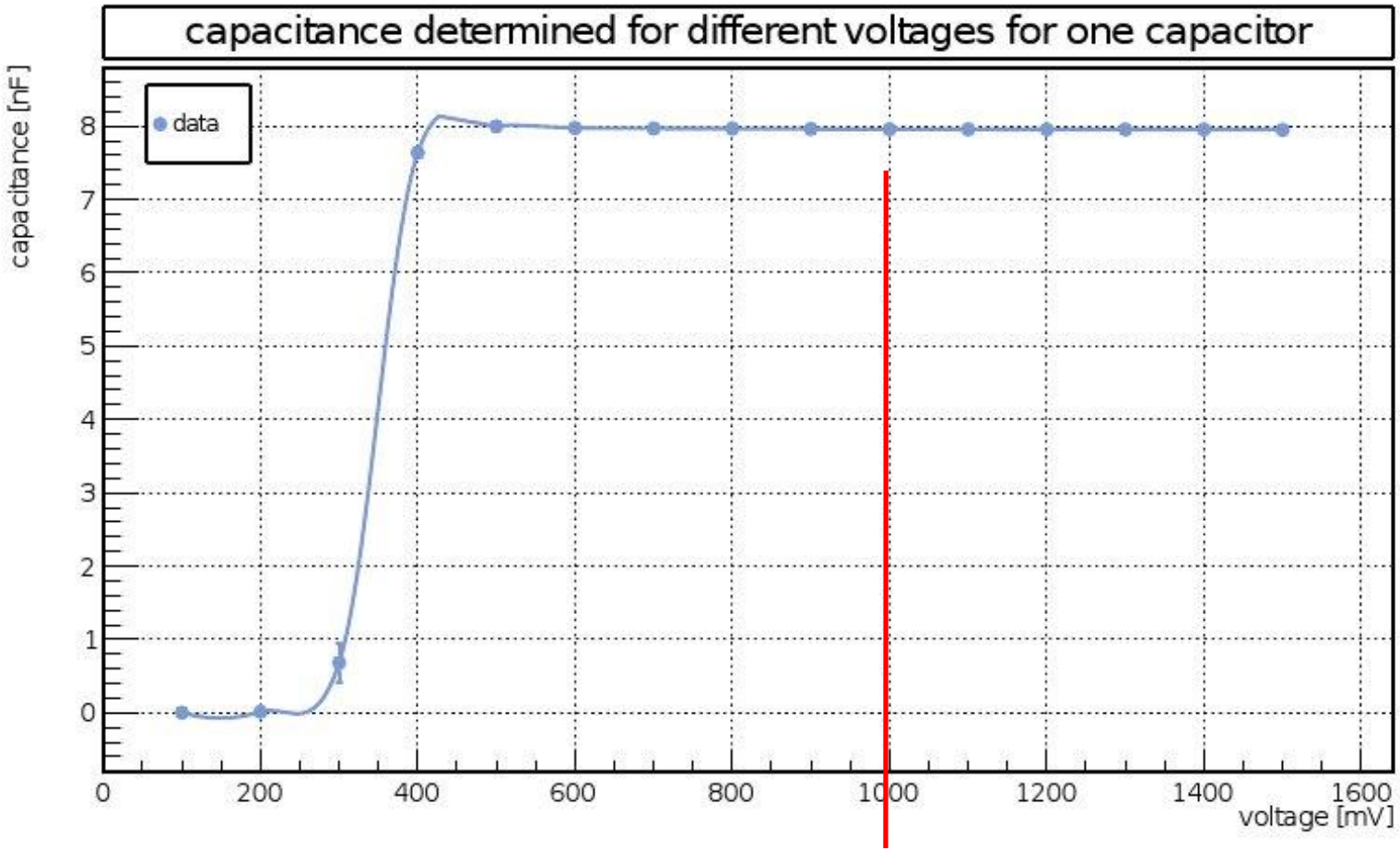
# Injection capacitance measurement I




$$C = \frac{1}{V_{cap}} \cdot \frac{I_{cap}}{f} = \frac{1}{1.0V} \cdot \frac{7.956\mu A}{MHz} = 7.96\,pF \;\rightarrow\; (C_{high} + C_{low}) = 7.96\text{fF}$$

- Simulated capacitance: 5.7 fF

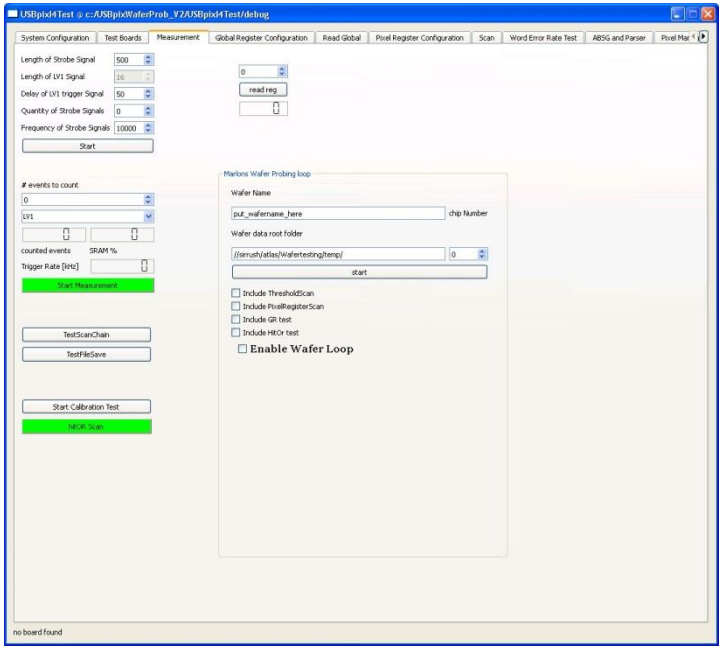
# Injection capacitance measurement




- In wafer probing: $U_{cap}$ = 1V by external power supply

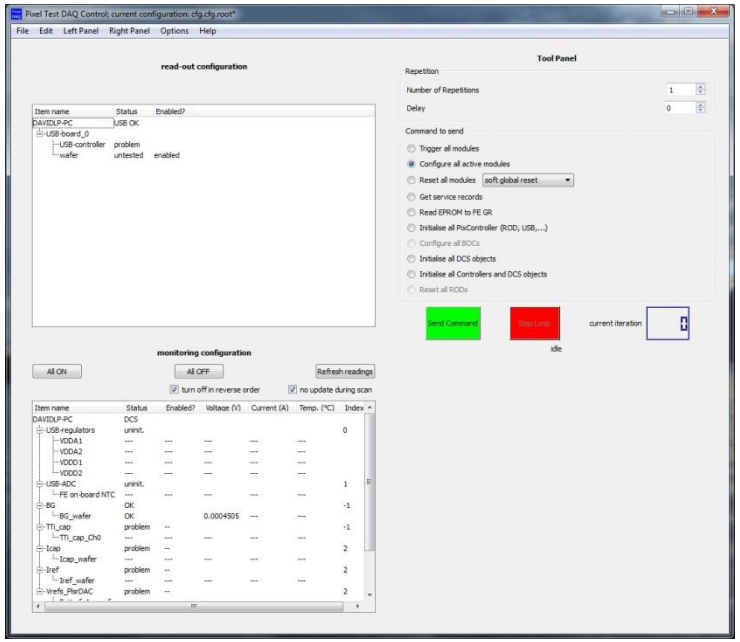
# From FE-I4A to FE-I4B wafer probing III

- New DAQ software for wafer testing: STcontrol




FE-I4A: USBpixTest based

→

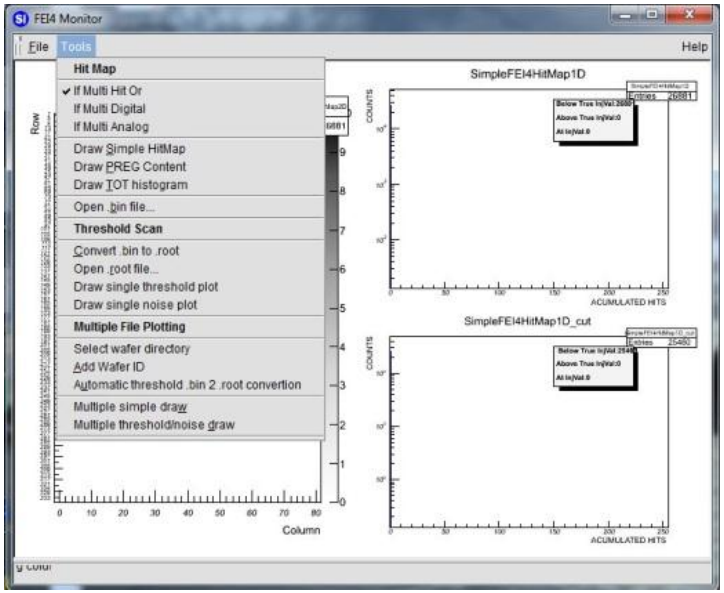



FE-I4B: STcontrol

- Reasons:
  - STControl provides more features: fitting, tuning, number of available scans, GPIB,…
  - Use the same DAQ software for test beams, 1-, 2-chip module testing and wafer analysis → same data format, better comparison of the results
- Status:
  - All scans work as expected
  - STControl showed stability issues → maybe related to file reading while probing
  - Serial number burning sometimes doesn‘t work for the LSB

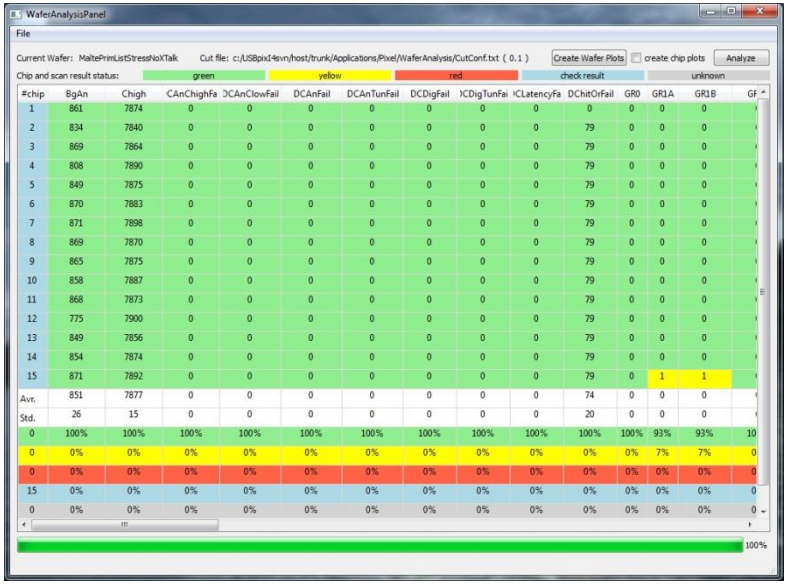
# From FE-I4A to FE-I4B wafer probing IV

- New analysis software: WaferAnalysis




FE-I4A: FE-I4 display

→




FE-I4B: WaferAnalysis

- Reasons:
  - More than 10 new scans on wafer level that have to be analyzed
  - It has to be fast and reliable
  - From 4 currents and voltages for FE-I4A to more than 100 currents (Scan Chain) and 9 voltages in FE-I4B wafer testing
  - → high level of automation needed
- Status:
  - >80% of the results can already be analyzed automatically
  - More statistic for the different values is needed to set cuts (green, yellow, red chip)

# STControl primitive List

- List is executed for each chip
- Takes approx. 48 min. per chip
- Abort conditions can be set
- Starts at index 0 and goes to 81
- Explanation for different items:

- Start chip in defined state
- Iref tuning
- Current consumption after power up
- Inj. capacitance measurement
- Global/pixel register test (2 min. / 10 min.)
- Scan chain tests
- Measure Current consumption after configuration

Shown on following slides

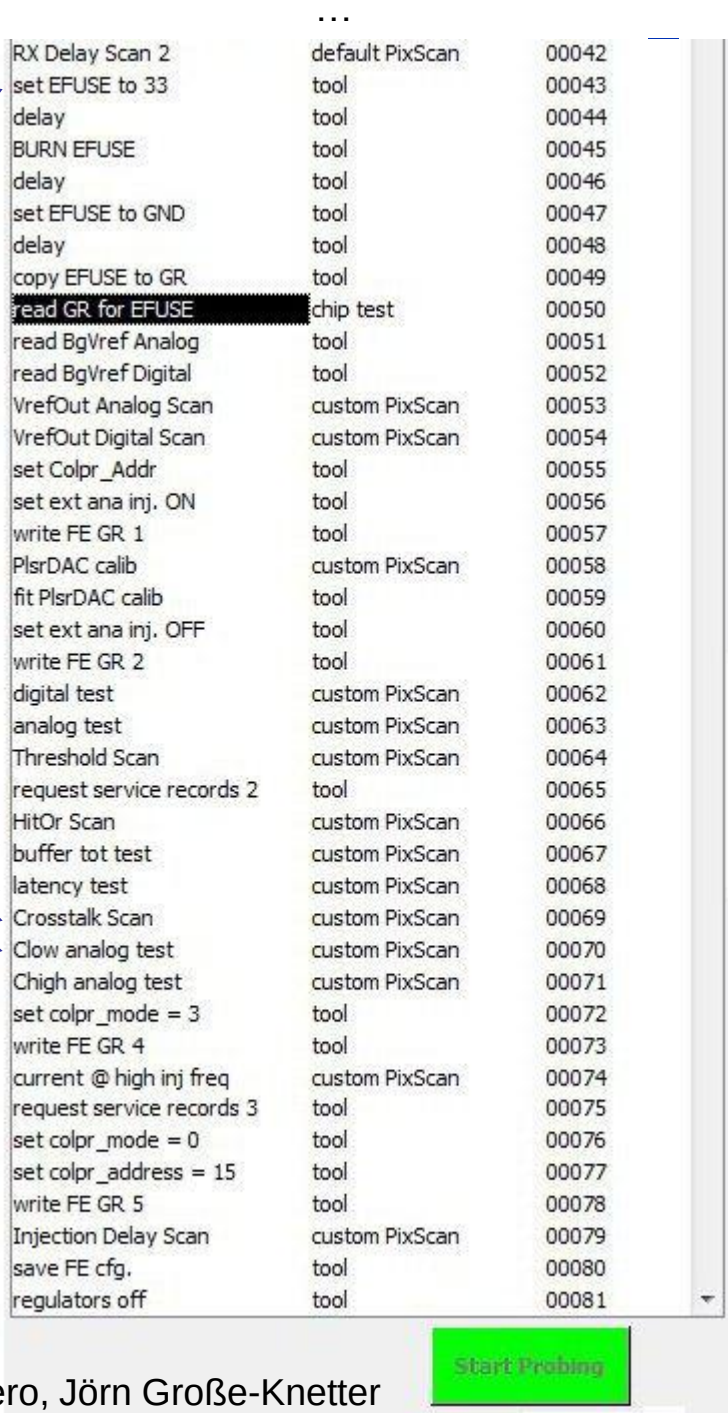
Primitive Items:

| Label | Type | Index |
|---|---|---|
| set EFUSE to GND | tool | 00000 |
| reload FE cfg. | tool | 00001 |
| set FE reset ON | tool | 00002 |
| regulators on | tool | 00003 |
| set FE reset OFF | tool | 00004 |
| set Iref measurement delay | tool | 00005 |
| switch open | tool | 00006 |
| Iref Scan | custom PixScan | 00007 |
| switch close | tool | 00008 |
| get best Iref at 2uA | tool | 00009 |
| read IDDD1 unconfig | tool | 00010 |
| read IDDA1 unconfig | tool | 00011 |
| read IDDD2 unconfig | tool | 00012 |
| read IDDA2 unconfig | tool | 00013 |
| RX Delay Scan | default PixScan | 00014 |
| turn TTi_cap on | tool | 00015 |
| set cap measurement delay | tool | 00016 |
| Cap calibration | custom PixScan | 00017 |
| turn TTi_cap off | tool | 00018 |
| set Cap value | tool | 00019 |
| GR test all 0 | chip test | 00020 |
| GR test all 1 A | chip test | 00021 |
| request service records 1 | tool | 00022 |
| GR test all 1 B | chip test | 00023 |
| GR test all 1 C | chip test | 00024 |
| GR test all 1 D | chip test | 00025 |
| GR test all 1 E | chip test | 00026 |
| GR test all 1 F | chip test | 00027 |
| PR test odd 1 | chip test | 00028 |
| PR test even 1 | chip test | 00029 |
| send hard reset | tool | 00030 |
| Scan Chain DOB | chip test | 00031 |
| send hard reset | tool | 00032 |
| Scan Chain CMD | chip test | 00033 |
| send hard reset | tool | 00034 |
| Scan Chain ECL | chip test | 00035 |
| send hard reset | tool | 00036 |
| configure FE | tool | 00037 |
| read IDDD1 after config | tool | 00038 |
| read IDDA1 after config | tool | 00039 |
| read IDDD2 after config | tool | |
| read IDDA2 after config | tool | |

# STControl primitive List

- Chip serial number burning
- Measure analog/digital bandgap reference
- Measure analog/digital Vrefs
- PlsrDAC transfer function measurement
- digital/analog test
- Threshold scan
- Hit Or scan configuration
- Buffer ToT test
- Latency test
- Crosstalk scan
- Clow/Chigh analog test
- Injection delay scan
- Save the scan config
- Power off

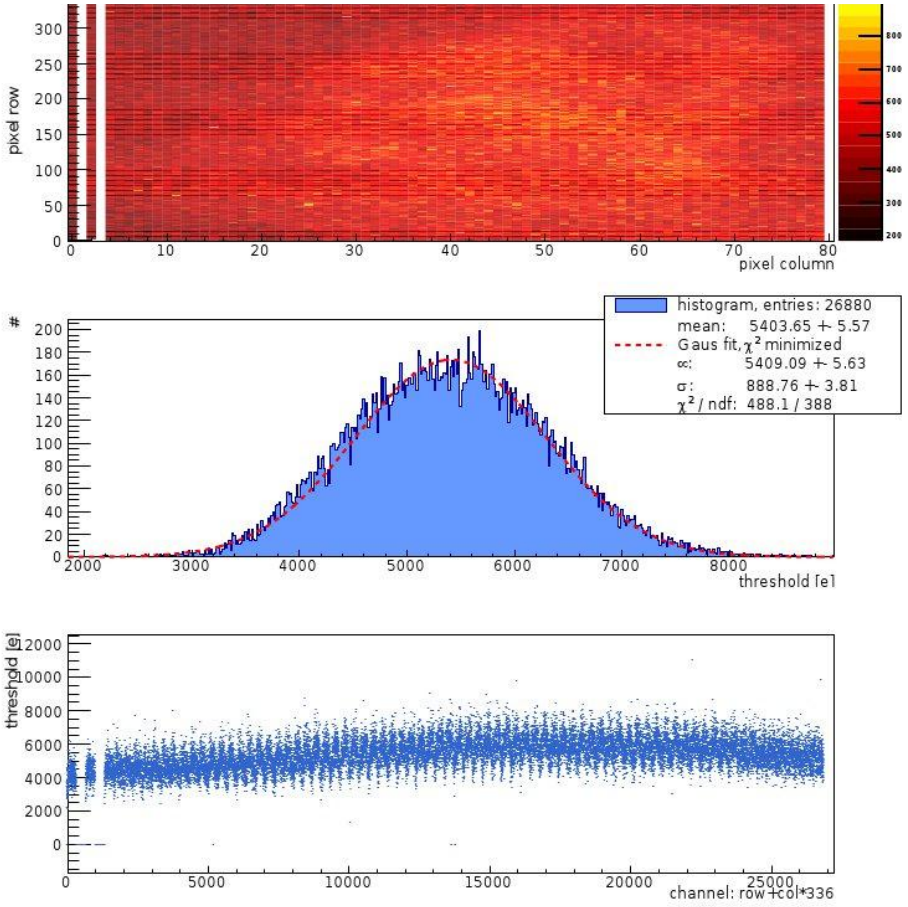
Shown on following slides



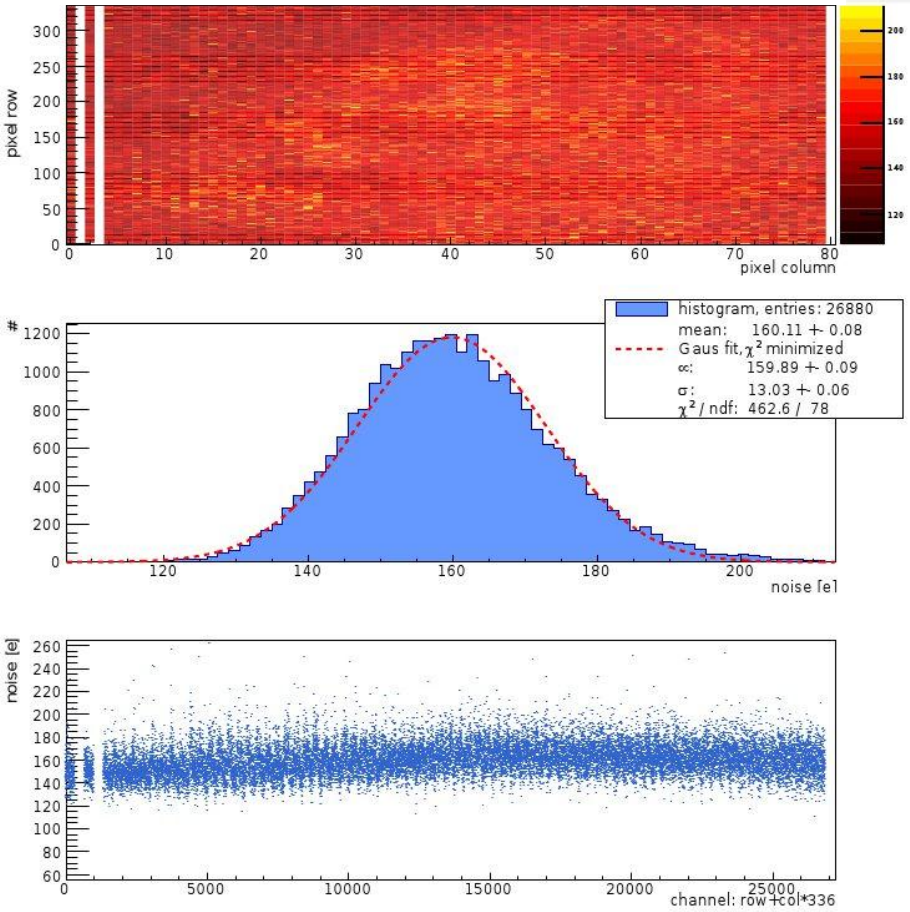
# Threshold scan on a FE-I4B wafer

Here: yellow chip and automatically created output from WaferAnalysis

threshold for chip 21




noise for chip 21



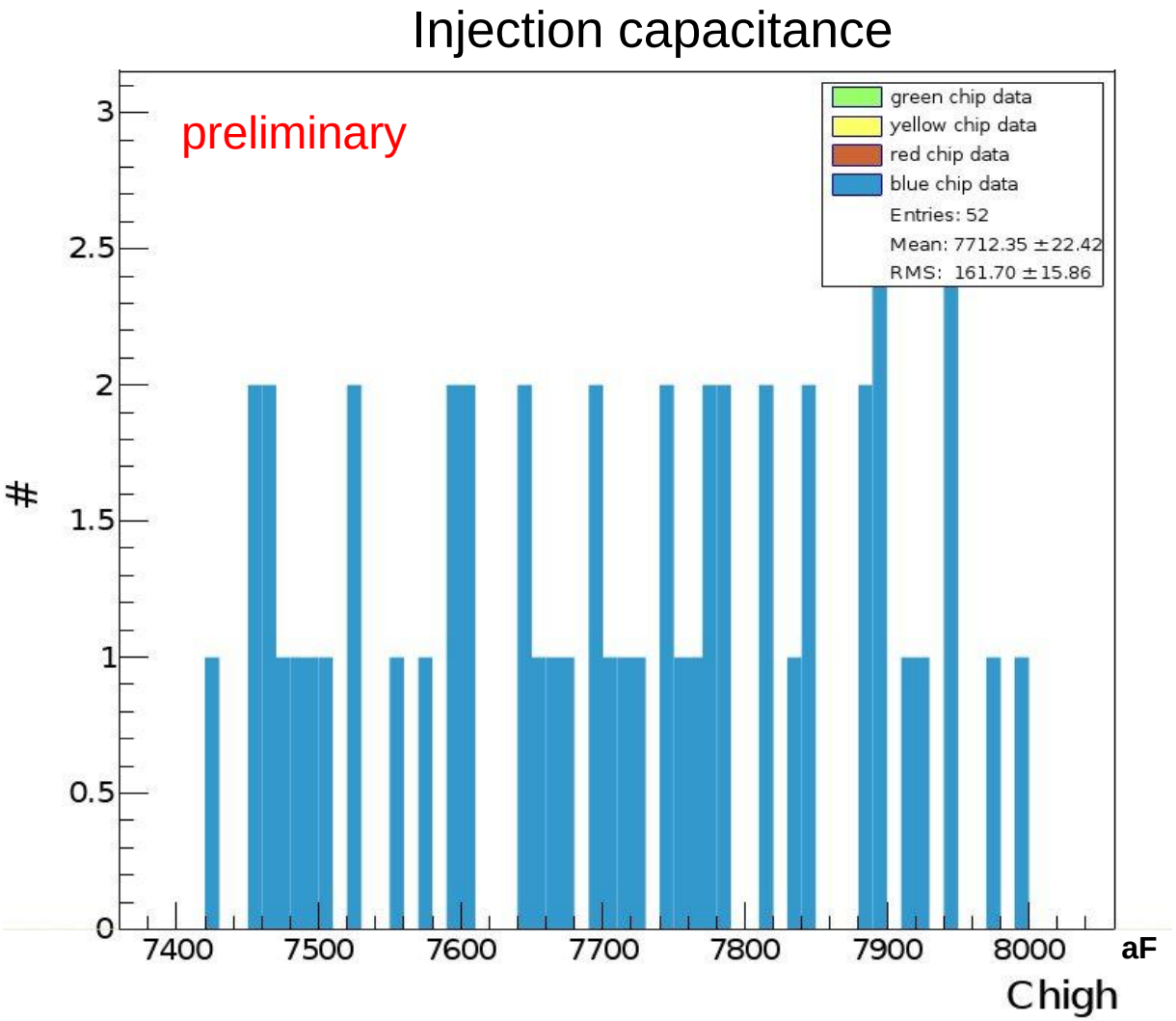

Threshold = 5400 e

Noise = 160 e

in the wafer probing setup not more noise than usual,
Note: inj. Cap. is here measured to be 7.7 fF (not 5.7 fF)

# Chigh+Clow distrib. on FE-I4B wafer

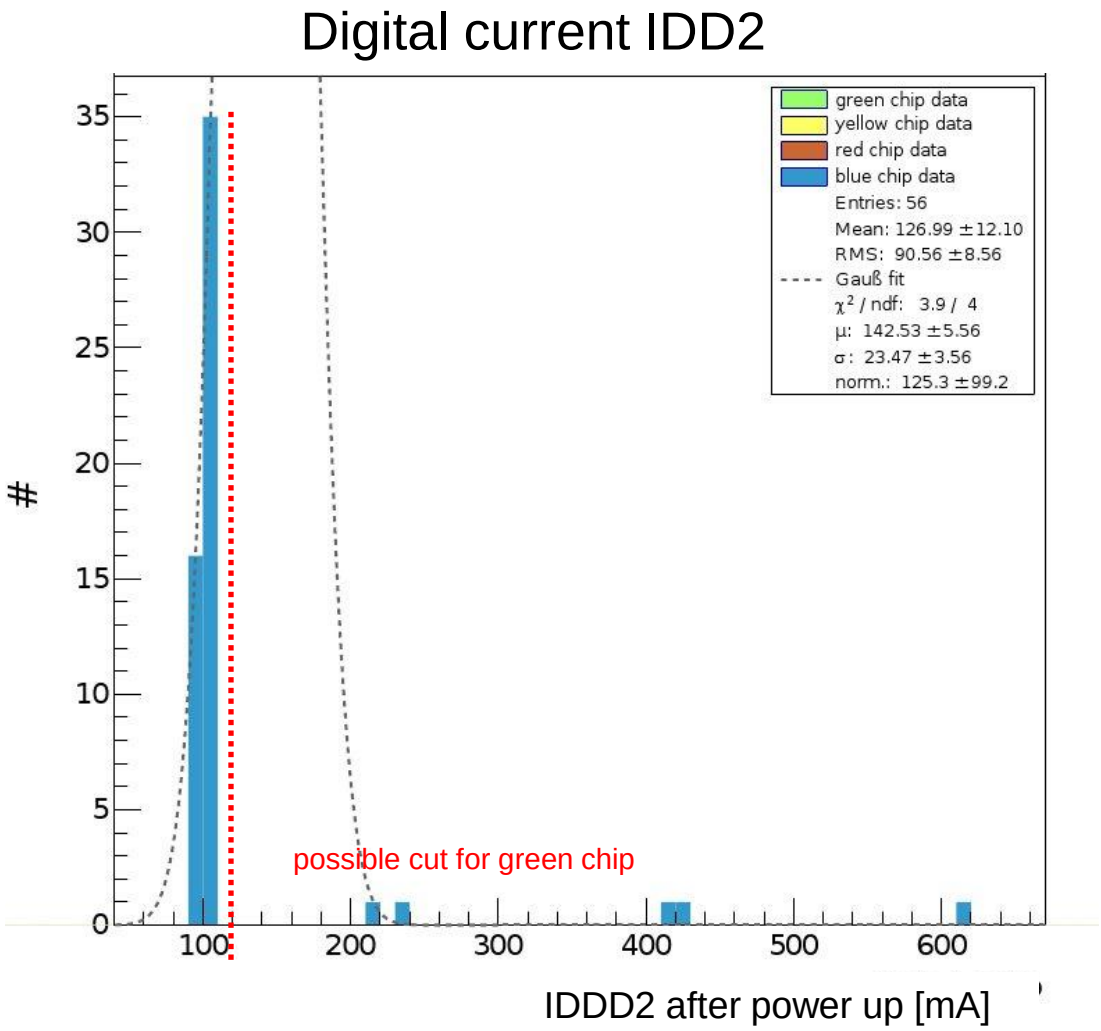
Here: 52 chips of one FE-I4B wafer and output by WaferAnalysis




Mean inj. Cap. measured on this FE-I4B wafer: 7.7 fF (simulation: 5.7 fF)

# Digital curr. distrib. on FE-I4B wafer

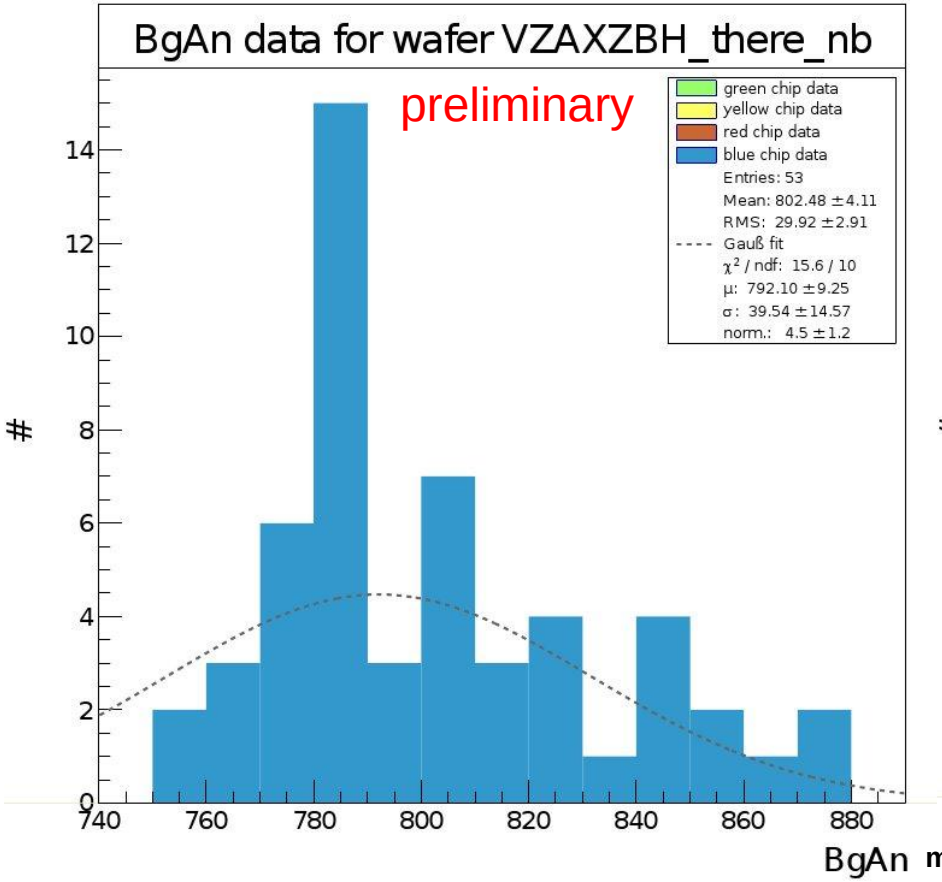
Here: 56 chips of one FE-I4B wafer and output by WaferAnalysis

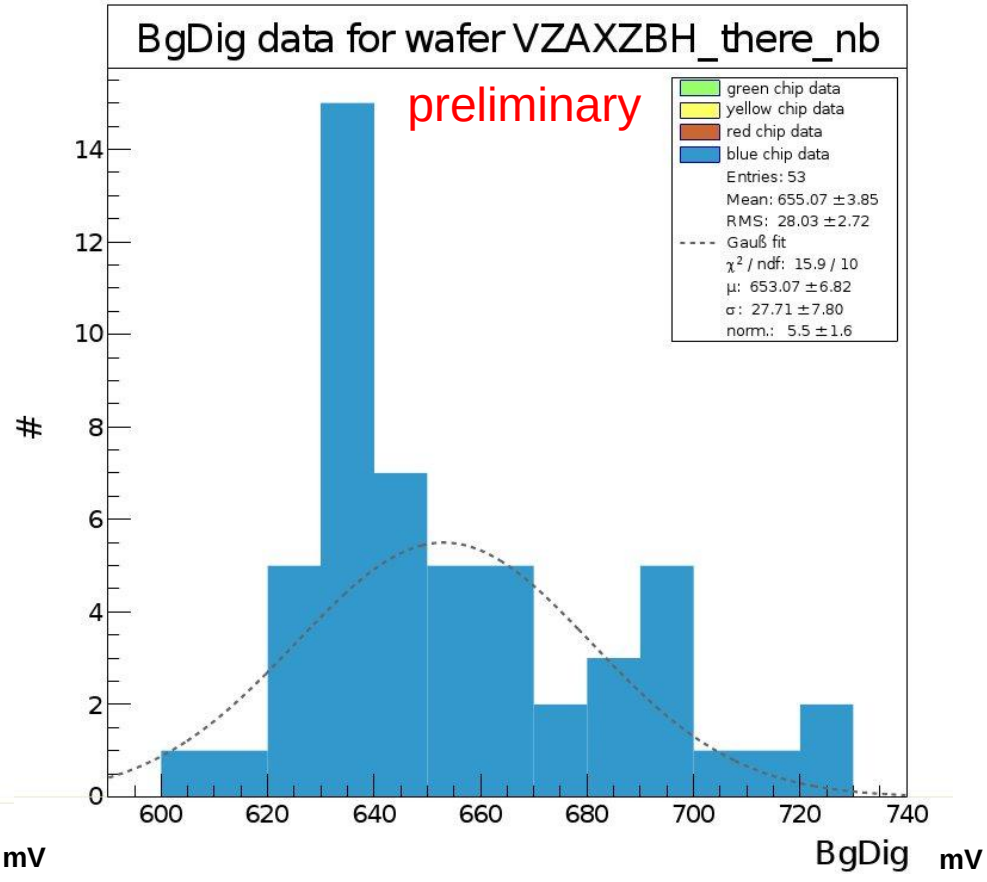



- Statistic will be collected for several wafers to be able to judge the results and to flag chip to be green, yellow or red

# Digital/Analog Band gap measurement

Here: 53 chips of one FE-I4B wafer and output by WaferAnalysis




- Band gap voltages and digital/analog Vrefs can be used as a regulator input
- Digital/analog voltage references (Vrefs) data is also available, but no analysis done yet

# Summary and outlook

## Summary:

- first FE-I4B wafer is almost probed (4 chips missing)
- results for the first 56 probed chips were shown
- to probe one chip takes ca. 48 min. → wafer takes ca. 2 days (if everything works smoothly)
- Stcontrol stability issues (hanging program) is probably related to an operating error
- Serial number  only partially or not burned

## Outlook:

- Understand and fix the serial number issue
- STcontrol stability will be checked on the next wafers
- To judge the state of a chip (green, yellow, red) a higher number of statistic is necessary, especially for the new scans
- (Automatic) upload to the IBL database

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# Backup slides…

# Wafer testing setup: proof of concept on the desk

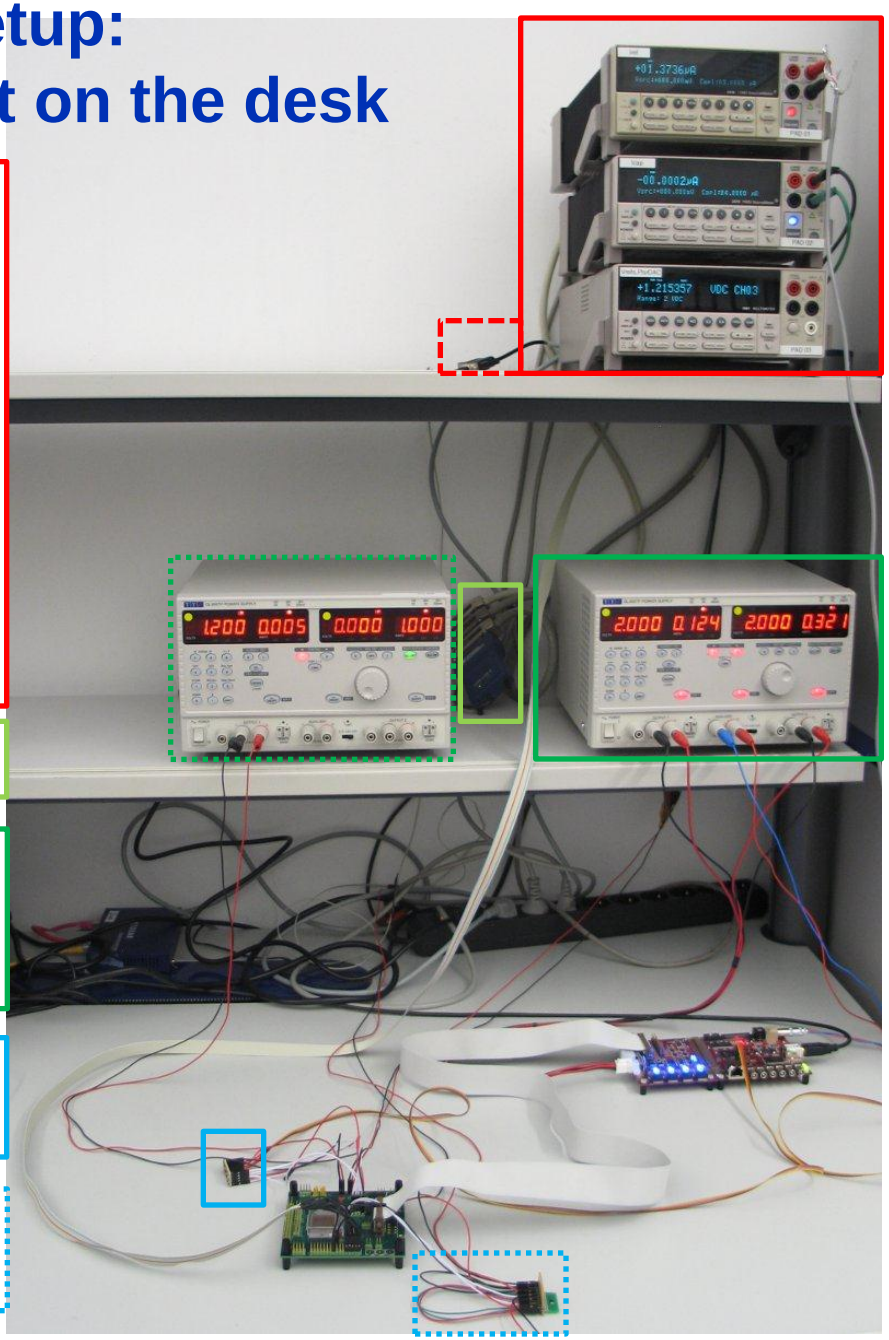
- Keithley 2410 for Iref curr. meas.
- Keithley 2410 for Icap curr. meas.
- Keithley 2001 + 2000 scanner card for
  - Voltage measurement:
    - VrefOutDig
    - VrefOutAn
    - BgVrefDg
    - BgVreAn
    - PlsrDac
  - Switch on/off Iref switch via digital I/O

- National Instrument USB-GPIB-B adapter

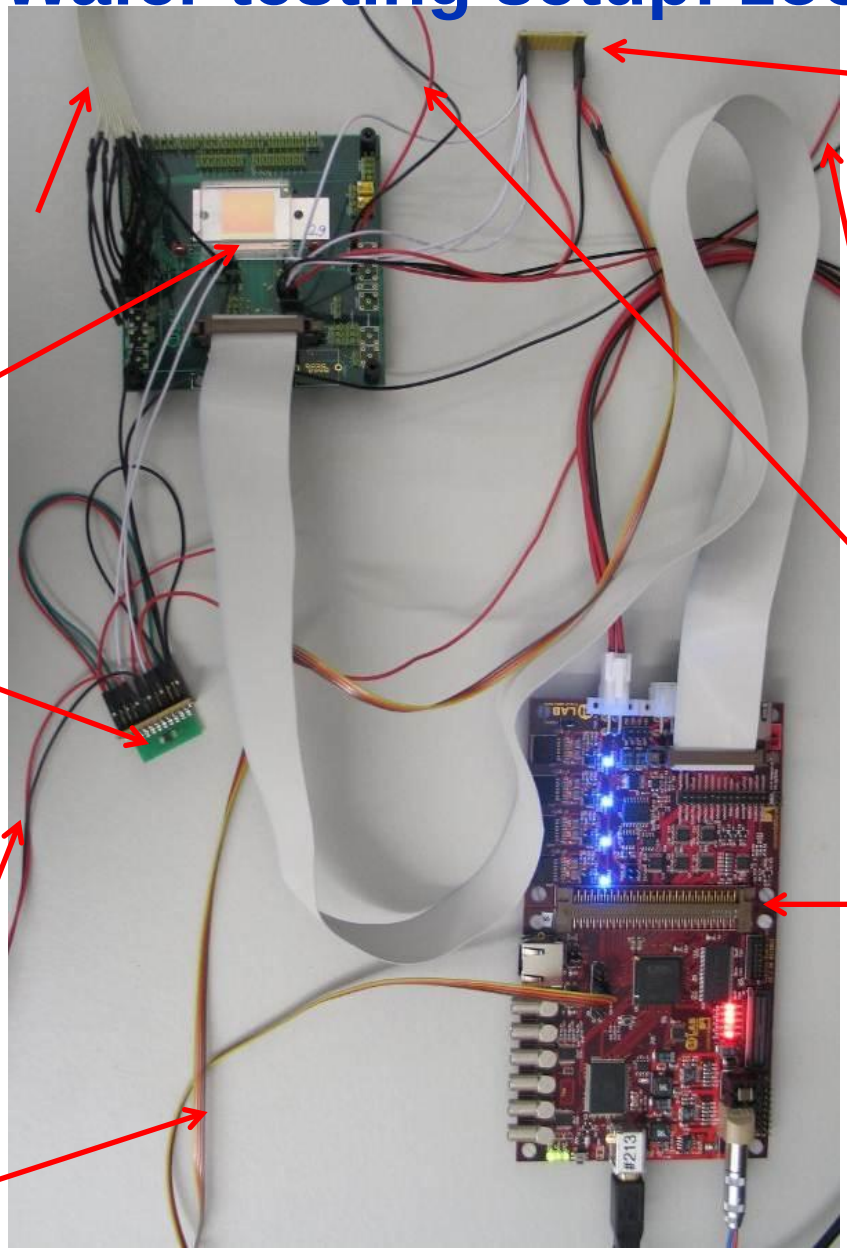
- TTi QL355TP power supply for regulators and multi-IO board
  + one TTi for cap measure?

- 4-channel single throw 3.3V switch to control Iref pads via multi-IO board

- In test setup: external Dual SPDT analog switch (switch is integrated on needle card)



# Wafer testing setup: zoom



10 wires flat cable to switcher card for voltage measurements

SCC FE-I4B

Dual SPDT analog switch

Twisted pair shielded cable to Iref source meter (cannot be Seen here…)

4 wires flat cable for Iref select

4 channel single throw 3.3V switch

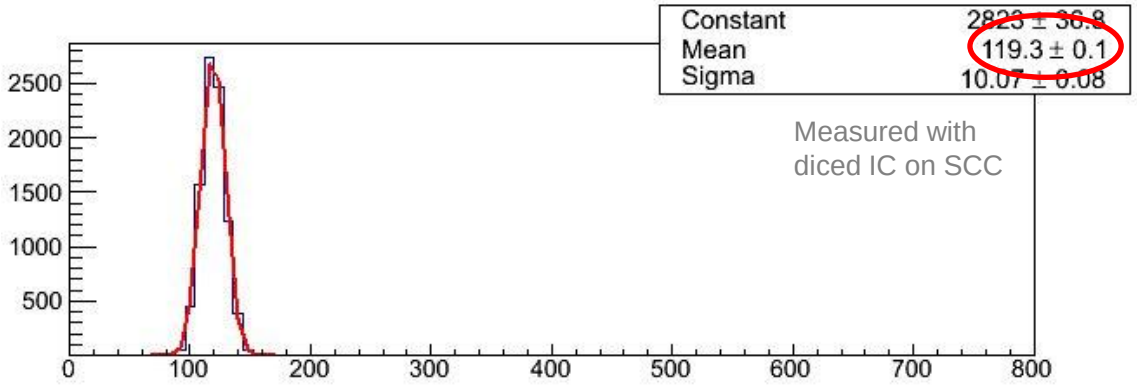
2 wires to digital I/O for switch switching

2 wires to Icap multimeter

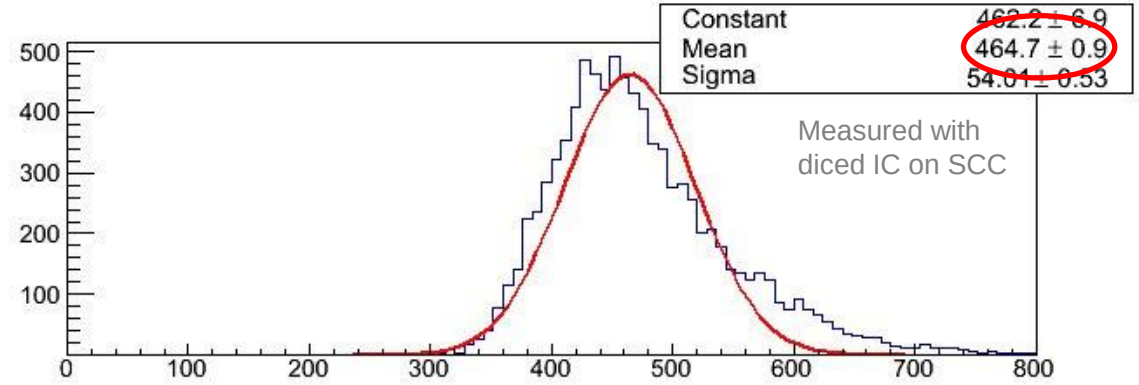
USBpix hardware

# Switch on PCB for Iref measurement

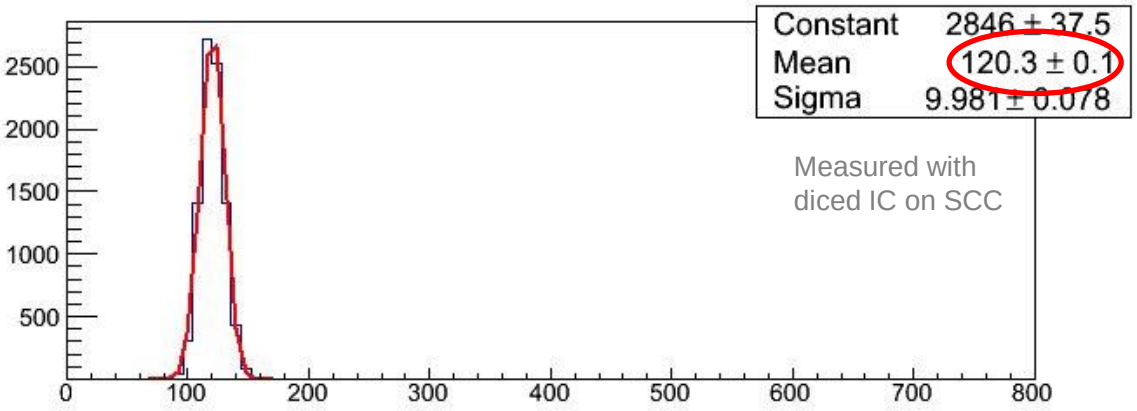
FE is very sensitive to any noise coupled to the Iref




no multimeter at Iref pin




multimeter at Iref pin
and switch opened for
Iref measurement




multimeter at Iref pin
and switch closed

# Buffer ToT test

Here: yellow chip of FE-I4B wafer and output by Stcontrol DataViewer

- Test the 5 hit storage of every pixel for every ToT value