

# **FE-I4B wafer probing**

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# **FE-I4A wafer probing summary**

- 20 FE-I4A wafers fully probed (80% Bonn, 20% Berkeley)
- 2 unprobed wafers for diced chips
- 4 at Aptasic
- 14 unprobed FE-I4A wafers in Bonn
- Time needed per wafer for one run: 35 h
- Yield of green chips:  $(69 \pm 3)\%$



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### From FE-I4A to FE-I4B wafer probing I

Many new things to do at wafer level (written in red)

Chip testing:

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- Current consumption after power up and after configuration
- Scan chain tests for 3 peripheral digital logic blocks (DOB, CMD, ECL)
- Analog/digital scan
- Latency counter test (in each PDR)
- Global and pixel register tests
- Analog/digital band gap references, analog/digital Vrefs from Iref
- Buffer ToT test (for each pixel)
- Hit Or test
- threshold scan
- analog/digital scan
- Clow/Chigh analog scan
- Crosstalk scan
- Current @ high trigger frequency test
- Injection delay scan
- Service records
- Chip calibration on wafer level:
  - Reference current tuning
  - Pulser DAC transfer function
  - Injection capacitance measurement
  - Measurement of the digital/analog band gap and digital/analog voltage references
  - 15-bit serial number burning: chip number (6-bit), wafer number (9-bit)

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# From FE-I4A to FE-I4B wafer probing II

- Hardware:
  - FE-I4B requires new PCB with new needle card
  - Extended hardware setup to:
    - Tune the reference current
    - Measure the PlsrDAC transfer function
    - Measure the digital/analog band gap references
    - Measure the tunable analog/digital references

    - Trigger the chip serial number burning
  - Shown on following slides



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#### Current reference (Iref) tuning



In FE-I4B: reference current can only be changed by Iref Pads
 → no access with the module flex

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### Injection capacitance measurement I



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# universitätbonn Injection capacitance measurement



• In wafer probing: U<sub>cap</sub> = 1V by external power supply

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# From FE-I4A to FE-I4B wafer probing III

• New DAQ software for wafer testing: STcontrol

and the second state of th	pixl4Test/debug	🔄 Pixet Test DAQ Control: current configuration: cfg.cdg.root*
Configuration Test Boards Measurement	Global Register Configuration Read Global Pixel Register Configuration Scan Word Error Rate Test ABSG and Parser Pixel Mar 🕑	File Edit Left Panel Right Panel Options Help
of Strobe Signal 500 \$ of LV1 Signal 16 \$ fLV1 trigger Signal 50 \$	e entre entr	read-out configuration Tool Panel           Tool Panel           Number of Expections         1
af to trapped spare and an	Verrere Verrer	Image: Statute Dealed: Discretion: good of the statute of depiction: good of the statute of
round		

FE-I4A: USBpixTest based

FE-I4B: STcontrol

- Reasons:
  - STControl provides more features: fitting, tuning, number of available scans, GPIB,...
  - Use the same DAQ software for test beams, 1-, 2-chip module testing and wafer analysis → same data format, better comparison of the results
- Status:
  - All scans work as expected
  - STControl showed stability issues → maybe related to file reading while probing
  - Serial number burning sometimes doesn't work for the LSB

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# From FE-I4A to FE-I4B wafer probing IV

 $\rightarrow$ 

• New analysis software: WaferAnalysis



FE-I4A: FE-I4 display

Current V	Vafer: MaltePr	imListStressNo	XTalk Cut f	le: c:/USBpixI4svi	n/host/trunk/A	pplications/Pixel/V	VaferAnalysis,	CutConf.txt (	0.1) Cn	eate Wafer Plo	ts 🔳	create chi	plots	Analyze
hip and :	scan result sta	tus:	green		yelo	N	n	ed		heck result	_		unknown	
#chip	BgAn	Chigh	CAnChighFa	DCAnClowFail	DCAnFail	DCAnTunFail	DCDigFail	)CDigTunFai	<b>ICLatencyFa</b>	DChitOrFail	GR0	GR1A	GR1B	GF
1	861	7874	0	0	0	0	0	0	0	0	0	0	0	
2	834	7840	0	0	0	0	0	0	0	79	0	0	0	
3	869	7864	0	0	0	0	0	0	0	79	0	0	0	
4	808	7890	0	0	0	0	0	0	0	79	0	0	0	
5	849	7875	0	0	0	0	0	0	0	79	0	0	0	
6	870	7883	0	0	0	0	0	0	0	79	0	0	0	
7	871	7898	0	0	0	0	0	0	0	79	0	0	0	
8	869	7870	0	0	0	0	0	0	0	79	0	0	0	
9	865	7875	0	0	0	0	0	0	0	79	0	0	0	
10	858	7887	0	0	0	0	0	0	0	79	0	0	0	
11	868	7873	0	0	0	0	0	0	0	79	0	0	0	
12	775	7900	0	0	0	0	0	0	0	79	0	0	0	
13	849	7856	0	0	0	0	0	0	0	79	0	0	0	
14	854	7874	0	0	0	0	0	0	0	79	0	0	0	
15	871	7892	0	0	0	0	0	0	0	79	0	1	1	
Avr.	851	7877	0	0	0	0	0	0	0	74	0	0	0	
Std.	26	15	0	0	0	0	0	0	0	20	0	0	0	
0	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	93%	93%	10
0	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	7%	7%	0
0	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0
15	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0
0	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0
•		311												+

FE-I4B: WaferAnalysis

- Reasons:
  - More than 10 new scans on wafer level that have to be analyzed
  - It has to be fast and reliable
  - From 4 currents and voltages for FE-I4A to more than 100 currents (Scan Chain) and 9 voltages in FE-I4B wafer testing
  - $\rightarrow$  high level of automation needed
- Status:
  - >80% of the results can already be analyzed automatically
  - More statistic for the different values is needed to set cuts (green, yellow, red chip)

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### universitätbonn STControl primitive List

- List is executed for each chip
- Takes approx. 48 min. per chip
- Abort conditions can be set
- Starts at index 0 and goes to 81
- Explanation for different items:
- Start chip in defined state
- Iref tuning
- Current consumption after power up
- Inj. capacitance measurement
- Global/pixel register test (2 min. / 10 min.)
- Scan chain tests
- Measure Current consumption after configuration

#### Shown on following slides

Label	Туре	Index	
set EFUSE to GND	tool	00000	
reload FE cfg.	tool	00001	
set FE reset ON	tool	00002	
regulators on	tool	00003	
set FE reset OFF	tool	00004	
set Iref measurement delay	tool	00005	
switch open	tool	00006	
Iref Scan	custom PixScan	00007	
switch close	tool	00008	
get best Iref at 2uA	tool	00009	
read IDDD 1 unconfig	tool	00010	
read IDDA1 unconfig	tool	00011	
read IDDD2 unconfig	tool	00012	
read IDDA2 unconfig	tool	00013	
RX Delay Scan	default PixScan	00014	
turn TTi_cap on	tool	00015	
set cap measurement delay	tool	00016	
Cap calibration	custom PixScan	00017	
turn TTi_cap off	tool	00018	
set Cap value	tool	00019	
GR test all 0	chip test	00020	
GR test all 1 A	chip test	00021	
request service records 1	tool	00022	
GR test all 1 B	chip test	00023	
GR test all 1 C	chip test	00024	
GR test all 1 D	chip test	00025	
GR test all 1 E	chip test	00026	
GR test all 1 F	chip test	00027	
PR test odd 1	chip test	00028	
PR test even 1	chip test	00029	
send hard reset	tool	00030	
Scan Chain DOB	chip test	00031	
send hard reset	tool	00032	
Scan Chain CMD	chip test	00033	
send hard reset	tool	00034	
Scan Chain ECL	chip test	00035	
send hard reset	tool	00036	
configure FE	tool	00037	
read IDDD1 after config	tool	00038	
read IDDA1 after config	tool	00039	
read IDDD2 after config	tool		
read IDDA2 after config	tool		

Primitive Items:

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# universitätbonn STControl primitive List

- Chip serial number burning
- Measure analog/digital bandgap reference
- Measure analog/digital Vrefs
- PIsrDAC transfer function measurement
- digital/analog test
- Threshold scan
- Hit Or scan configuration
- Buffer ToT test
- Latency test
- Crosstalk scan
- Clow/Chigh analog test
- Injection delay scan
- Save the scan config
- Power off



RX Delay Scan 2	default PixScan	00042
set EFUSE to 33	tool	00043
delay	tool	00044
BURN EFUSE	tool	00045
delay	tool	00046
set EFUSE to GND	tool	00047
delay	tool	00048
copy EFUSE to GR	tool	00049
read GR for EFUSE	chip test	00050
read BgVref Analog	tool	00051
read BgVref Digital	tool	00052
VrefOut Analog Scan	custom PixScan	00053
VrefOut Digital Scan	custom PixScan	00054
set Colpr_Addr	tool	00055
set ext ana inj. ON	tool	00056
write FE GR 1	tool	00057
PlsrDAC calib	custom PixScan	00058
fit PlsrDAC calib	tool	00059
set ext ana inj. OFF	tool	00060
write FE GR 2	tool	00061
digital test	custom PixScan	00062
analog test	custom PixScan	00063
Threshold Scan	custom PixScan	00064
request service records 2	tool	00065
HitOr Scan	custom PixScan	00066
buffer tot test	custom PixScan	00067
latency test	custom PixScan	00068
Crosstalk Scan	custom PixScan	00069
Clow analog test	custom PixScan	00070
Chigh analog test	custom PixScan	00071
set colpr_mode = 3	tool	00072
write FE GR 4	tool	00073
current @ high inj freq	custom PixScan	00074
request service records 3	tool	00075
set colpr_mode = 0	tool	00076
set colpr_address = 15	tool	00077
write FE GR 5	tool	00078
Injection Delay Scan	custom PixScan	00079
save FE cfg.	tool	00080
regulators off	tool	00081

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#### Threshold scan on a FE-I4B wafer

Here: yellow chip and automatically created output from WaferAnalysis



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LOW

pixel



in the wafer probing setup not more noise than usual, Note: inj. Cap. is here measured to be 7.7 fF (not 5.7 fF)

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Injection capacitance



Mean inj. Cap. measured on this FE-I4B wafer: 7.7 fF (simulation: 5.7 fF)

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• Statistic will be collected for several wafers to be able to judge the results and to flag chip to be green, yellow or red

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### Digital/Analog Band gap measurement

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- Band gap voltages and digital/analog Vrefs can be used as a regulator input
- Digital/analog voltage references (Vrefs) data is also available, but no analysis done yet

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#### Summary:

- first FE-I4B wafer is almost probed (4 chips missing)
- results for the first 56 probed chips were shown
- to probe one chip takes ca. 48 min.  $\rightarrow$  wafer takes ca. 2 days (if everything works smoothly)
- Stcontrol stability issues (hanging program) is probably related to an operating error
- Serial number only partially or not burned

#### **Outlook:**

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- Understand and fix the serial number issue
- STcontrol stability will be checked on the next wafers
- To judge the state of a chip (green, yellow, red) a higher number of statistic is necessary, especially for the new scans
- (Automatic) upload to the IBL database



Backup slides...

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10 wires flat cable to switcher card for voltage measurements

SCC FE-I4B

Dual SPDT analog switch

Twisted pair shielded cable to Iref source meter (cannot be Seen here...) 4 wires flat cable for Iref select

#### Wafer testing setup: zoom

4 channel single throw 3.3V switch

2 wires to digital I/O for switch switching

2 wires to Icap multimeter

USBpix hardware

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#### Switch on PCB for Iref measurement

FE is very sensitive to any noise coupled to the Iref



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- Test the 5 hit storage of every pixel for every ToT value

ToT0 mod 0 bin 0 chip 0

