universitätbonn

Wafer probing setup for FE-I4B

- Setup
- Proof of concept measurements

Setup (hardware)

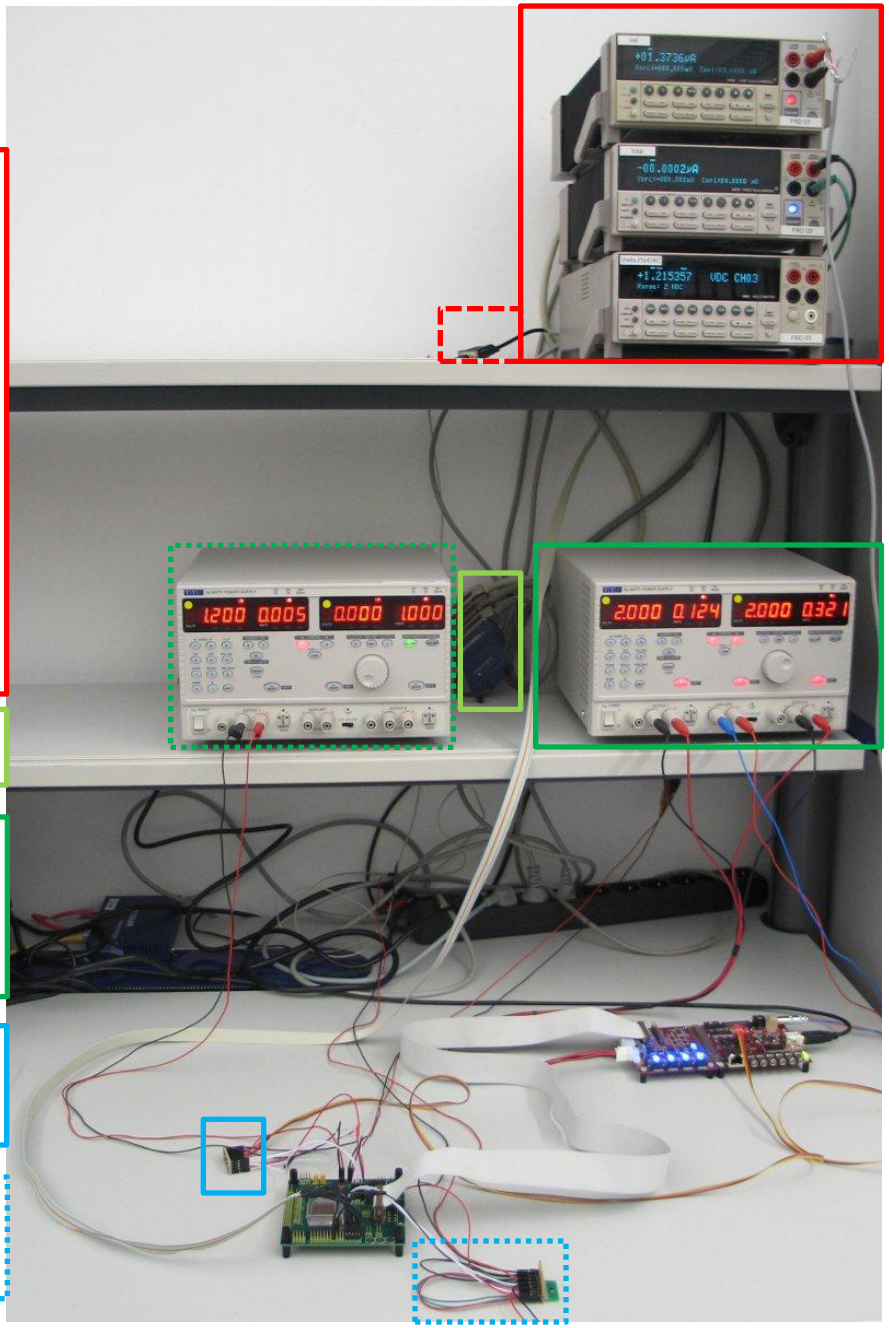
- Keithley 2410 for Iref curr. meas.
- Keithley 2410 for Icap curr. meas.
- Keithley 2001 + 2000 scanner card for
  - Voltage measurement:
    - VrefOutDig
    - VrefOutAn
    - BgVrefDg
    - BgVreAn
    - PlsrDac
  - Switch on/off Iref switch via digital I/O

- National Instrument USB-GPIB-B adapter

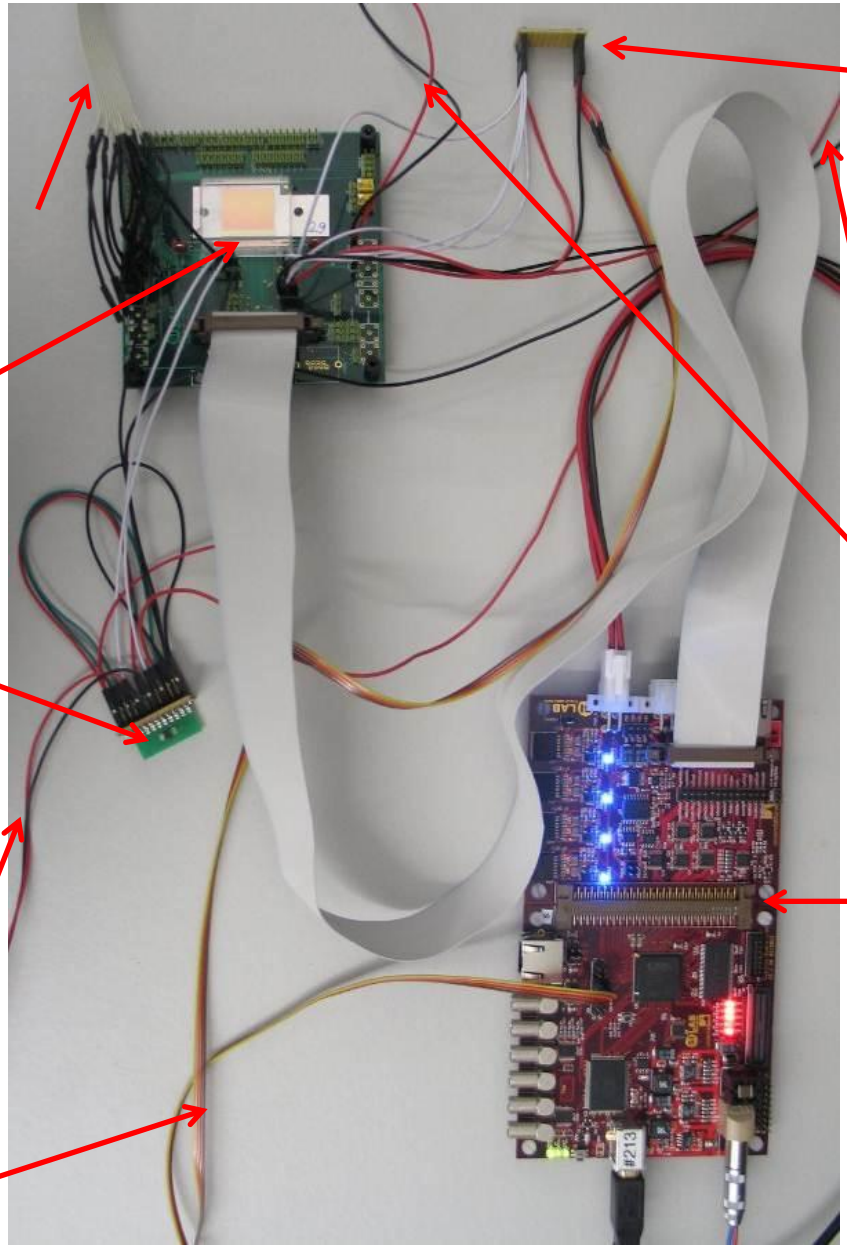
- TTi QL355TP power supply for regulators and multi-IO board
  + one TTi for cap measure?

- 4-channel single throw 3.3V switch to control Iref pads via multi-IO board

- In test setup: external Dual SPDT analog switch (switch is integrated on needle card)



Test setup zoom (hardware)



10 wires flat cable to switcher card for voltage measurements

SCC FE-I4B

Dual SPDT analog switch

Twisted pair shielded cable to Iref source meter

4 wires flat cable for Iref select

4 channel single throw 3.3V switch

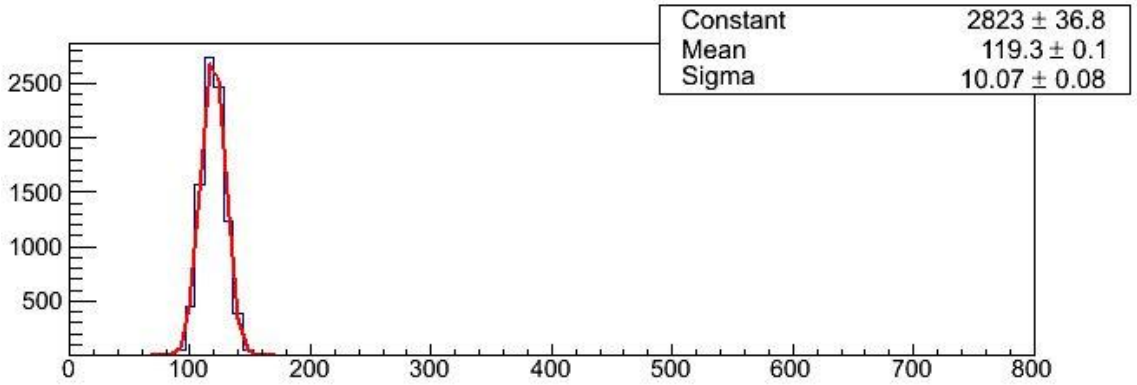
2 wires to digital I/O for switch switching

2 wires to Icap multimeter

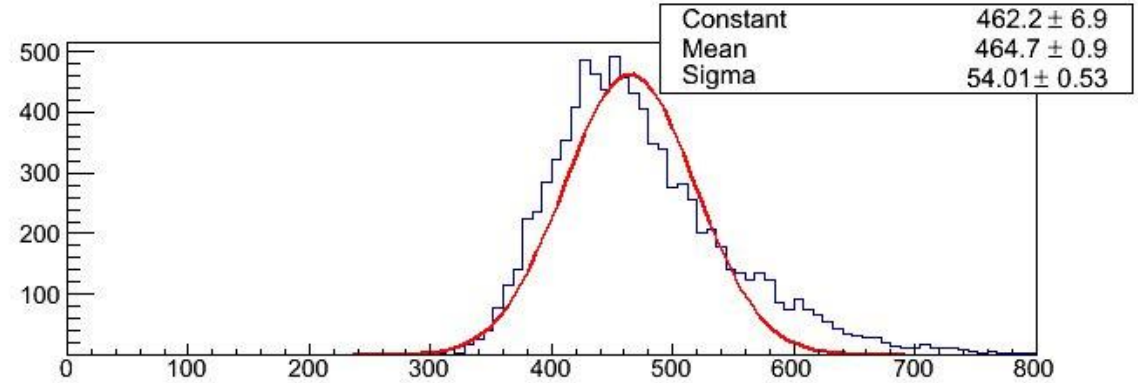
USBpix hardware

Why the switch for Iref measurement?

- FE is very sensitive to any noise coupled to the Iref

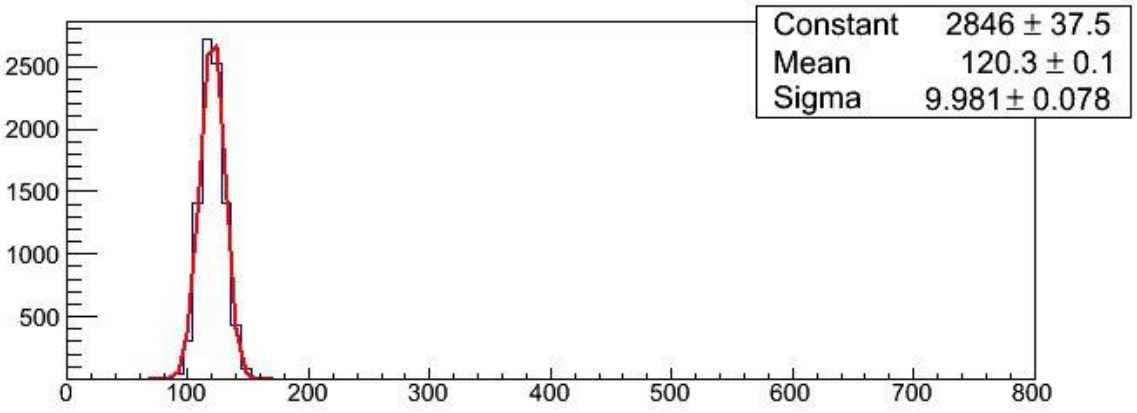


no multimeter at Iref pin



multimeter at Iref pin
and switch opened

depending on the multimeter and the cable up to +1000 e noise



multimeter at Iref pin
and switch closed

depending on the multimeter also more noise measured with switch closed

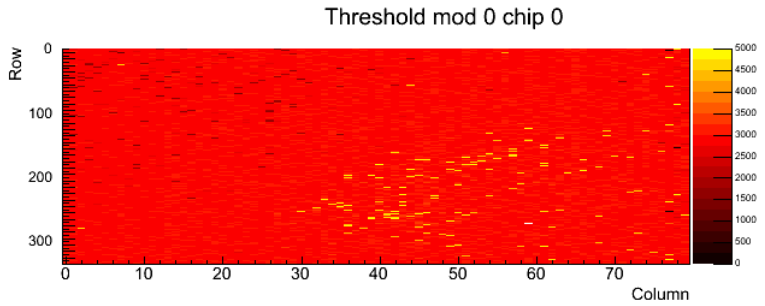
Setup (software)
STControl prim. list

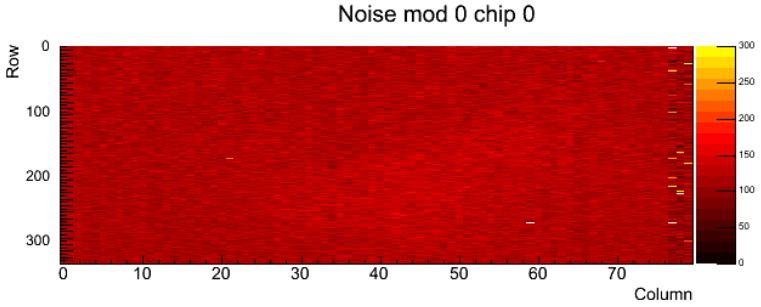
- RX delay scan
- Global/pixel register test (2 min. / 20 min.)
- Measure Current consumption after power up
- Scan reference current and set it to 2 uA
- Measure analog/digital bandgap reference
- Scan analog/digital voltage reference
- Scan Icap of cap. measurement circuit at different frequencies
- Scan pulser DAC function
- Digital/analog scan
- Threshold tuning
- Threshold scan
- HitOr scan (not working, not tested)
- Total time for this list: 36 min.
- Where EFUSE burning? → ID definition?
- Implement scan chain?
- Set measured injection capacitance?
- Abort conditions, 2nd run necessary?

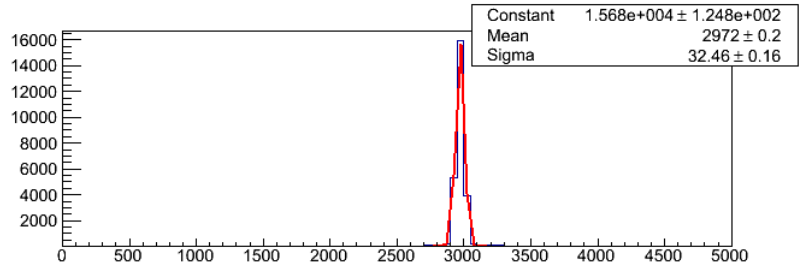
Primitive Items:

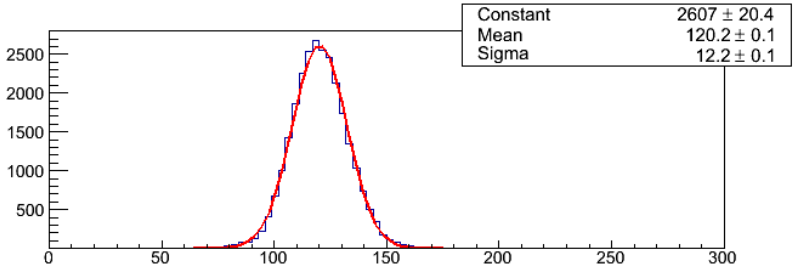
Label	Type	Index
reload FE cfg.	tool	00000
set FE reset ON	tool	00001
regulators on	tool	00002
set FE reset OFF	tool	00003
RX Delay Scan	default PixScan	00004
GR test all 0	chip test	00005
GR test all 1 A	chip test	00006
GR test all 1 B	chip test	00007
GR test all 1 C	chip test	00008
GR test all 1 D	chip test	00009
GR test all 1 E	chip test	00010
GR test all 1 F	chip test	00011
PR test all 0	chip test	00012
PR test all 1	chip test	00013
PR test all even rows 1	chip test	00014
PR test all odd rows 1	chip test	00015
configure FE	tool	00016
read IDDD1 after config	tool	00017
read IDDA1 after config	tool	00018
read IDDD2 after config	tool	00019
read IDDA2 after config	tool	00020
set Iref measurement delay	tool	00021
switch open	tool	00022
Iref Scan	custom PixScan	00023
switch close	tool	00024
get best Iref at 2uA	tool	00025
write FE GR 0	tool	00026
read BgVref Analog	tool	00027
read BgVref Digital	tool	00028
VrefOut Analog Scan	custom PixScan	00029
VrefOut Digital Scan	custom PixScan	00030
Icap Scan	custom PixScan	00031
set Colpr_Addr	tool	00032
set ext ana inj. ON	tool	00033
write FE GR 1	tool	00034
PlsrDAC calib	custom PixScan	00035
fit PlsrDAC calib	tool	00036
set ext ana inj. OFF	tool	00037
write FE GR 2	tool	00038
digital test	custom PixScan	00039
analog test	custom PixScan	00040
GDAC fast tune	custom PixScan	00041
write FE GR 3	tool	00042
TDAC fast tune	custom PixScan	00043
Threshold Scan	custom PixScan	00044
HitOr Scan	custom PixScan	00045
regulators off	tool	00046
save FE cfg.	tool	00047

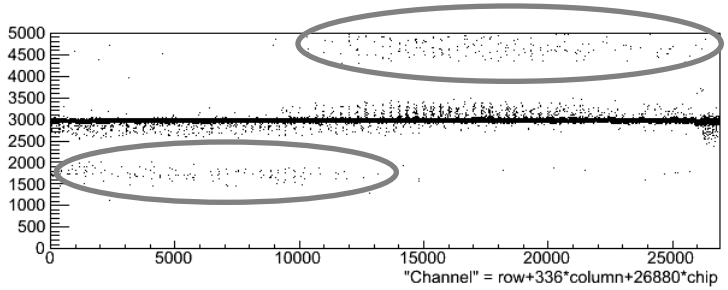
Threshold scan (theshold/noise plots)



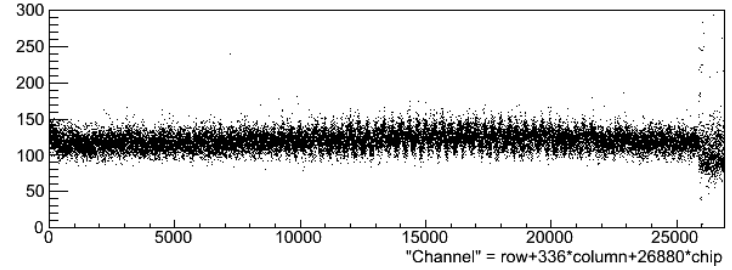








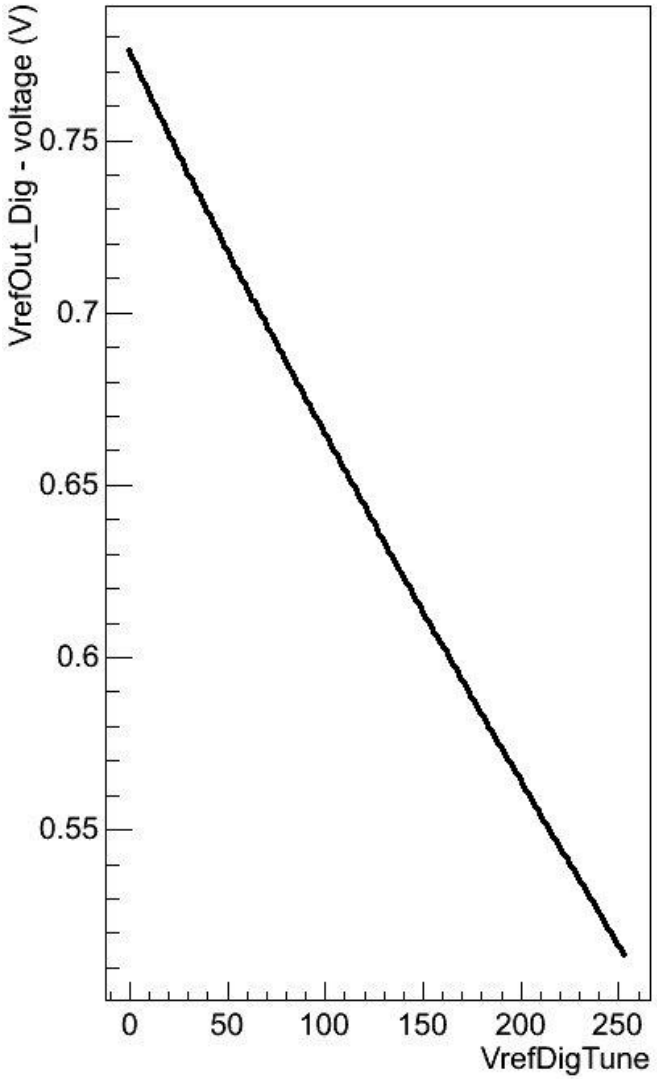
TDACVbp too low



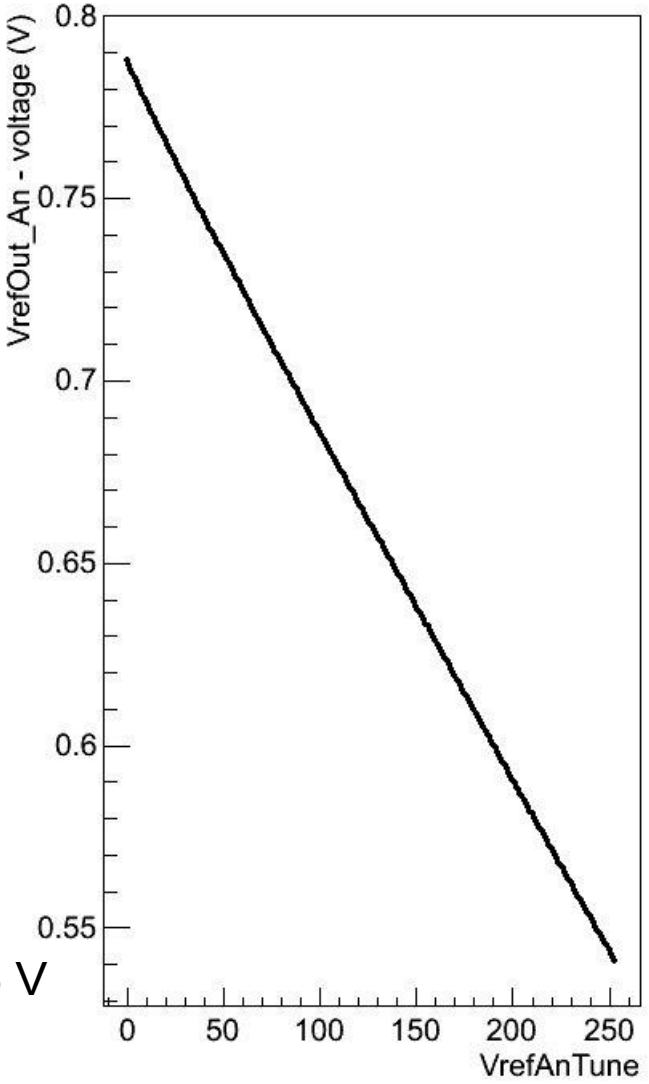
Standard DAC settings changed to get ca. 3000 e threshold and 15ke @ 5 ToT:

- PrmpVbpf = 180
- FDACVbn = 20
- VthinAF = 130
- TDACVbp = 120

Digital/Analog Vref tuning

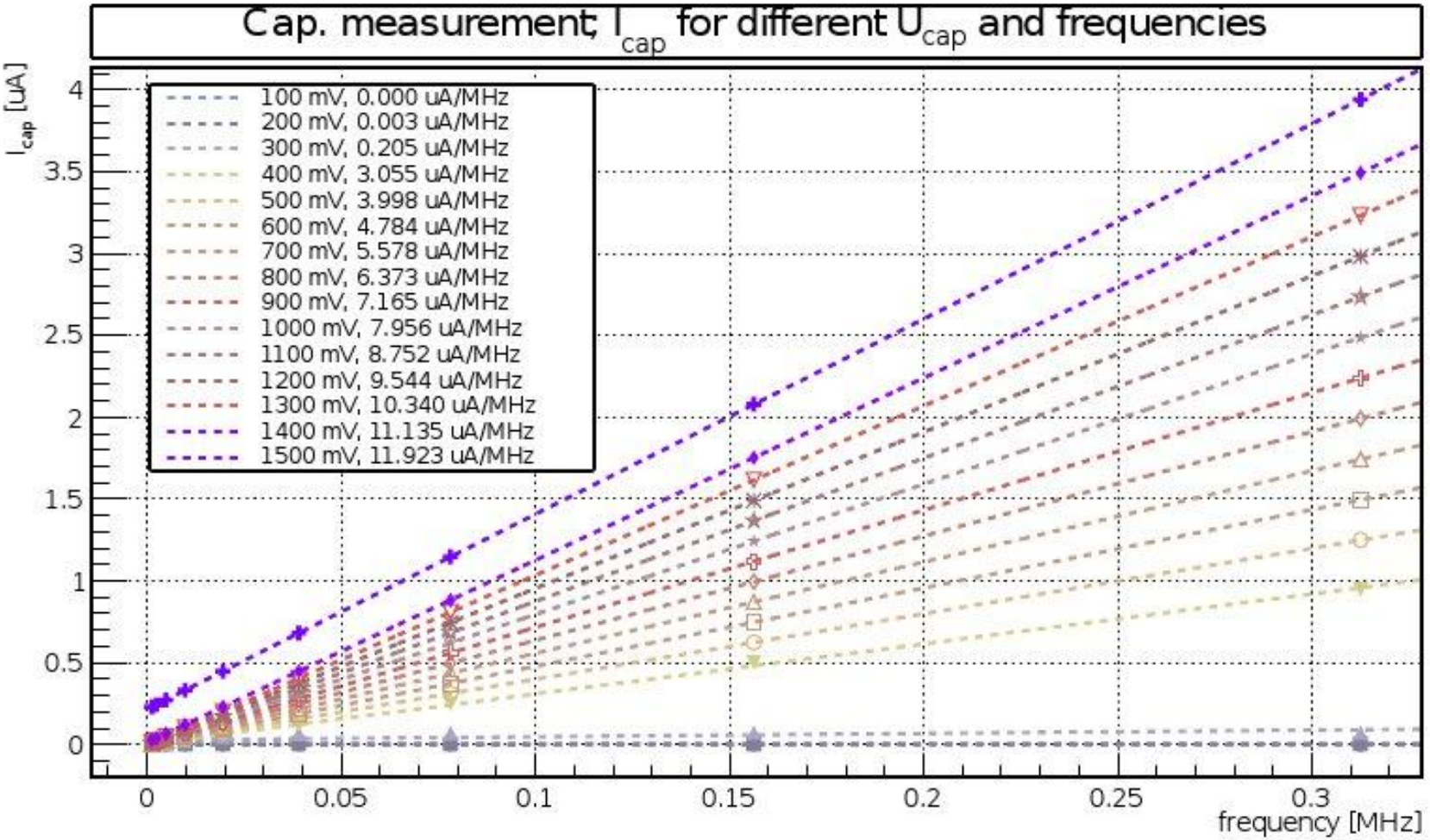


done with 1.5 V



To scan 254 DAC settings takes 40 s via GPIB → use less points to save time

Cap. Measurement



$$C = \frac{1}{V_{cap}} \cdot \frac{I_{cap}}{f} = \frac{1}{1.2V} \cdot \frac{9.544\mu A}{MHz} = 7.95\,pF \;\rightarrow\; (C_{high} + C_{low}) = 7.97\text{fF}$$

Why so high?

Summary and outlook

- ready to move to the probe station
- primitive list needs some extensions (EFUSE, …)
- on chip power regulation powering at wafer level?
- next revision of needle card with ADCs, switcher controllable via I^2C? To simplify the setup