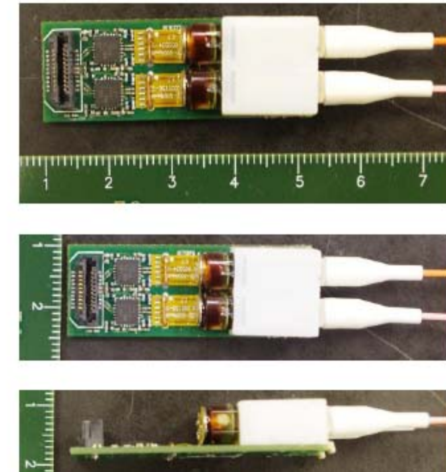
END of STAVE THERMAL FEA

(Barrel Stave 130)

- o Aim is to estimate effect of EoS chip heat on -
  - *Sensor: Temperature, Runaway Headroom*
  - *EoS: GBT chipset, VECSL temperatures*
- o TWO Phases of Interest, with different coolant temperatures, T_C :
  - *Operation:* $T_C \sim -30C$
  - *Stave Integration: tracker above dew-point (not closed):* $T_C \sim +15C$ *(45C higher!)*
- o Assume (for now) a Conventional Stave Core: Side Mounted Cards top and bottom.
  - *Focus on feasibility of a simplified cooling pipe*
- o "Speculative" Many of the FEA ingredients are **uncertain**!

EoS COMPONENTS - THERMAL



VTR: *Assume* physically similar to SMU design (Dual Tx for Calo):

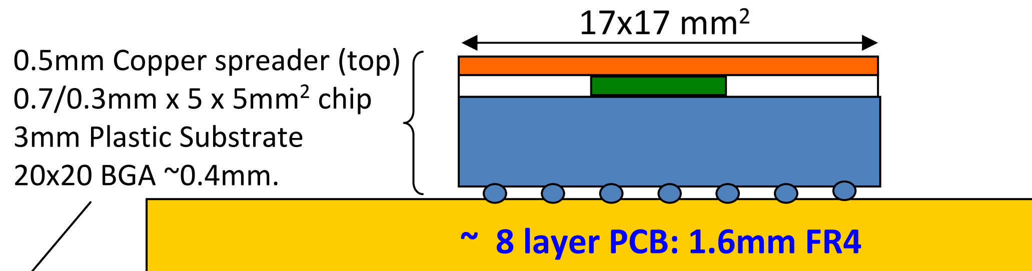
Transmitter: 217mW (LpGBLD 40% lower. Still in 130nm)

Receiver: 120mW (+ PIN diode ff. Rad.damage ?)

(? Jan Troska, AUW: "VTR doesn't need active cooling")

FEA: VTR NOT modelled thermally (only cosmetic)….
Inject VTR Heat into connector footprint.

GBT: 1.8W (Lp version - 65nm Schedule+Reliability issues.)
Package: ASE(Taiwan) via IMEC:



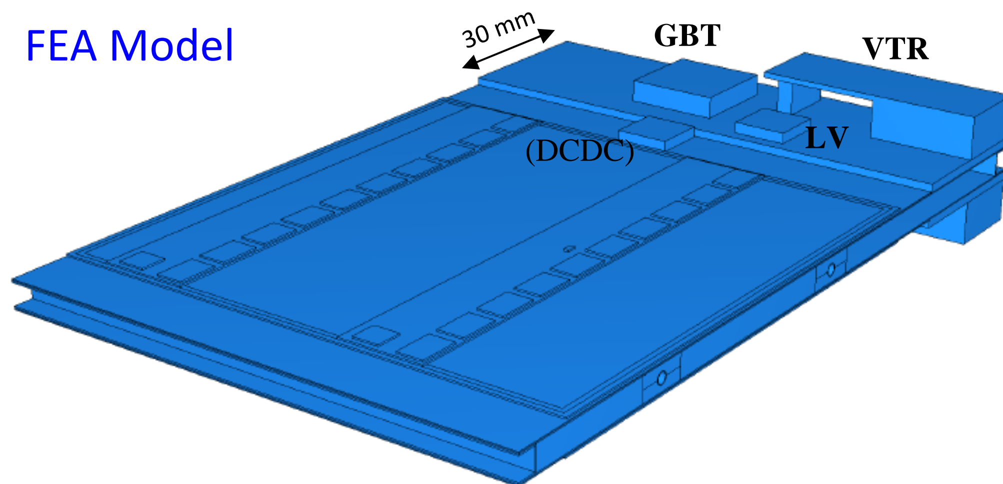
PCB:
Assume 2x17μm Cu planes
(! heat spreading near chip).
Thermal Vias: Not in FEA (needs design): could reduce ΔT by ×3?

Not final package? Thermal R (die => board) not known (aim to measure!).
FEA: Assume 10C/W (experience with Motorola MCP7447A ceramic). Model as isotropic, K = 1.4W/m-K.

Power Conversion: Useful Power 2.14W
Assume (aggressive) 75% efficiency => **0.7 W (conversion)**

Total SMC power (per face) 2.84W (equiv.to ~ ½ hybrid power)

FEA Model



Conduction to adjacent module is ~ 20%: neglected here.

LV and VTR are cosmetic only, apart from heat injected into PCB footprint! GBT *is* modelled, to have some estimate of die temperature.

DESY meeting: wider PCB (50mm?)

(For convenience have suppressed honeycomb volumes: were modelled as air)

CO_2 Temperature (Boundary Conditions) – refinement of previous FEA!

Pressure drop => Temperature drop of ~ 3C along pipe (will be measured at CERN).

- Mean fluid T is 1.5 degrees below input T. (=> correction to Runaway Headroom: now "23C wrt input fluid")
- Fluid T vs Z: ~ equal at Z=0, increasingly asymmetric towards EoS.

⇒ In presence of other sources of asymmetry, direction of flow matters!

NEAR End of Stave (but away from SMC): Temperature variation across Sensor.

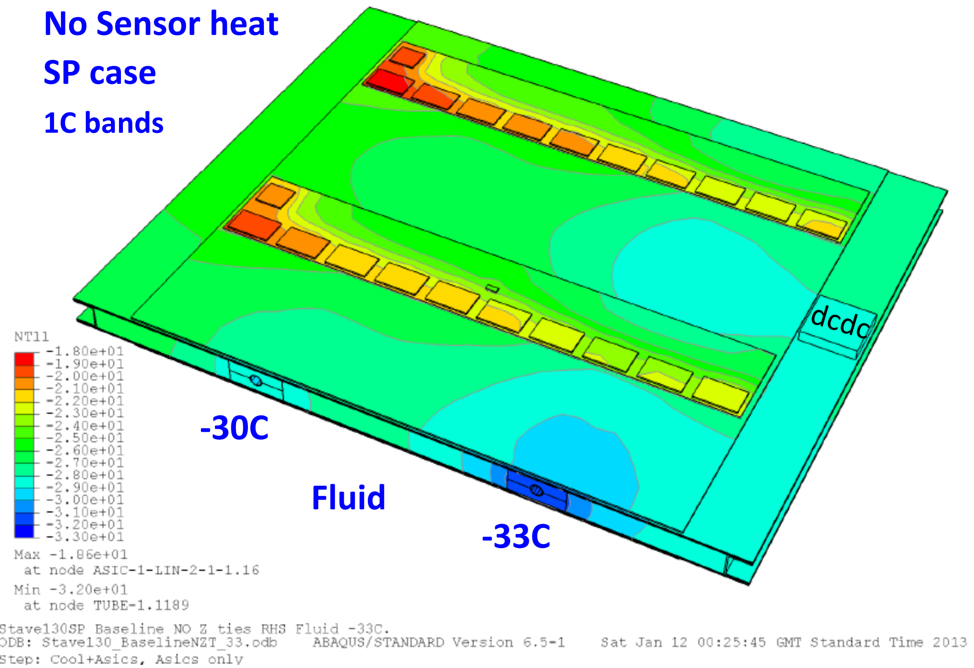
- No sensor heat (3000 fb^{-1},-25C expect ~ 0.4W)
- Hybrid heat 5.6W/module face (~1mW/chan).

Sensor T Variation due to:

- Hybrid/HCC/Pipe: 3.5C
- Asymmetric fluid T: 2C

gives for:

- **SP:** ~ **5.5** degrees over sensor area.
- **DCDC** (edge-mounted):
  - ~ **4 deg**. (fluid as shown) Preferred?
  - ~ **7 deg**. (flow reversed) Uncomfortable?



This perhaps sets the scale for acceptable level of T variation due to presence of SMC.

> *Note: The above FEA plot neglects heat flow between modules due to asymmetric hybrid placement.*
>
> *Hybrid placement affects the range of T variation across the sensor: IF symmetrically placed hybrids have become the baseline it would be an advantage to change the model to reflect that!*

Convection +Radiation - appreciable since the SMC and chips are at relatively high T.

- included crudely in the model as a surface film effect at the pcb surface (biggest contribution):

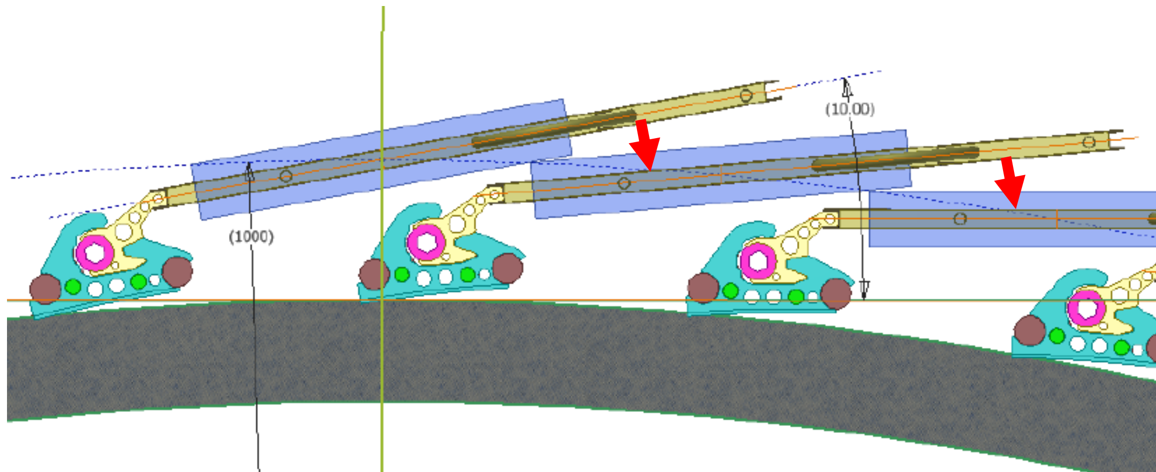
htc 10 W/m^{2}K ; ambient T -23.5C (approx. mean stave surface T).

- accounts for about 0.4W (15%) heat *loss* from the SMC.

- lowers the GBT chip T by typically 5C.

Where does the heat go?

At worst, it is a 0.5W load on the module below (<10% hybrid heat) - *Ignored in the FEA.*

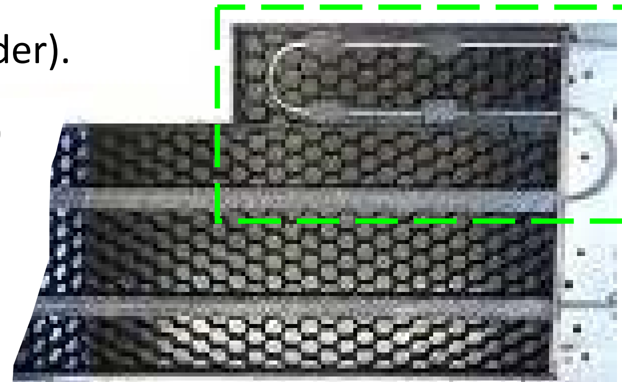


The Pipe “Wiggle” Issue:

To date, cooling pipe formed with a wiggle (meander).

- brings the coolant close to the SMC chips (good!)

- cools the sensor to below typical sensor T.



Several reasons to suppress / simplify this structure:

- Mechanical simplicity
- Avoid the loop outside stave end => close the gap between stave and barrel interlinks
- Reduce the Ti pipe length (avoids a weld?)
- *Operationally*: Avoid the associated pressure drop (note small radius bends) , *particularly* if located at *outlet* i.e. between the stave and the back pressure regulation.

=> Motivates cooling structure with straight pipes (or reduced meander) + passive conduction.

Result for Straight Pipes (no wiggle) – no additional conductive material in core.
! Fluid OUTlet (-33C) on SMC side.

Effect of SMC on the Sensor (SP case):

- T gradient (due to fluid) is reversed:

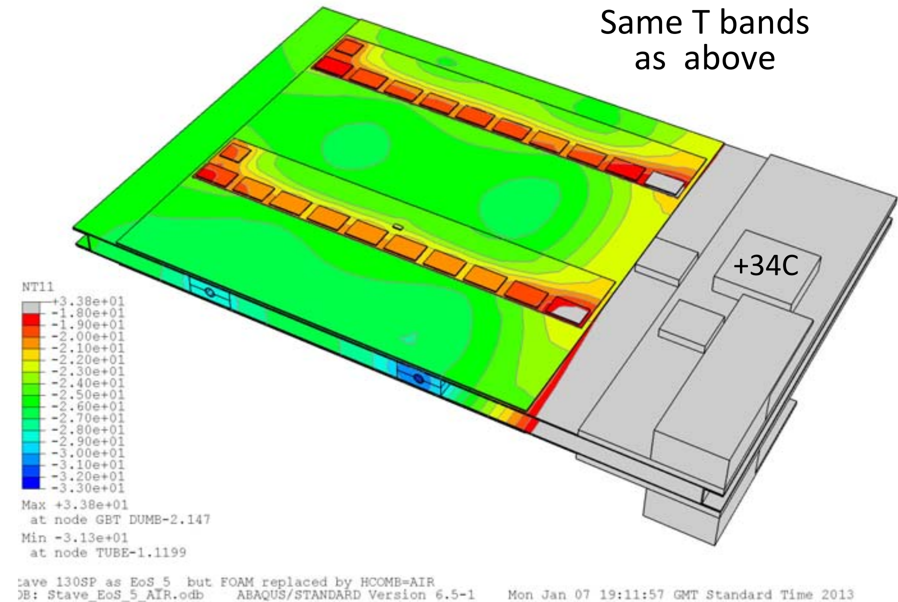
  => nett T variation = 5.5C (i.e. no worse)!

- Mean Sensor T raised by 1.9C, slightly lower R_T (SMC spreading?)

  => Runaway Headroom reduced by 1.5C (23=>21.5 degrees)

CONCLUDE: *With this direction of fluid flow, the effects of SMC heat on Runaway Headroom and nett Sensor T variation are small.*

=> Forget about the runaway aspect!
(Additional material and intelligent channelling of the SMC heat can only improve this).



- looks a lot better than I said at the AUW: largely due to lower assumed SMC power and the fluid asymmetry.

(Berlin NH Hotel napkin: "Inspiration can hit you at any time"…)

In the analytic approximation to runaway: A change in headroom due to a fixed ΔQ that raises the Sensor temperature by ΔT (in absence of leakage current), is equivalent to changing the coolant temperature by the same ΔT. (…true so long as the Sensor T Is fairly uniform). *(note Q_{hybrid} ~ 6W, Q_{SMC} ~ 3W).*

However…..

=> GBT chip temperature in above configuration is high: **+34C** (! 67 degrees above fluid T).
- Implies that during integration GBT sits at **+80C. (too high?).**

(Assuming pcb thermal vias, maybe +24C (opn.), +70C (intgn) - Still too high?).

FEA: run pipe directly under GBT => +11C => **Lateral heat xfer to straight pipe costs 23 degrees**.

Not enough Lateral conduction!

Compare: CFRP: 0-90-0 100gsm K13D2U, 140W/mK * 0.21mm => 30 [W.mm/mK]

…or, much worse (need to measure!): 45gsm K13C2U expect 10 ?

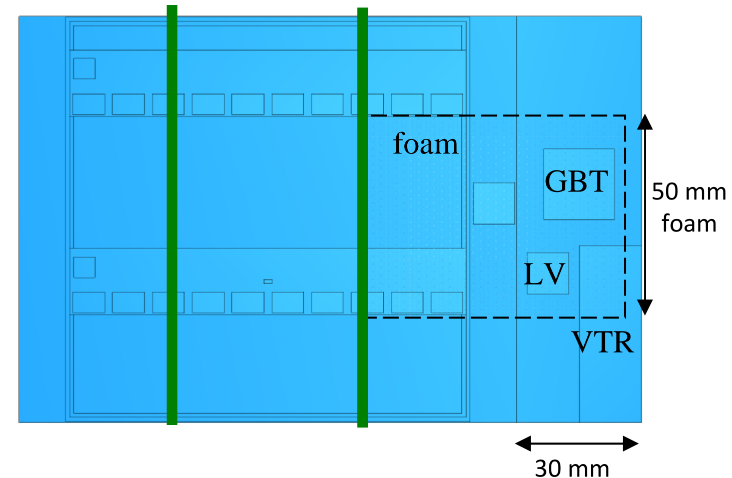
Try: Replace honeycomb by Allcomp Foam (ρ 0.25 g/cm^3), 30W/mK *2mm 60.

=> Add foam 56mm <X> x 50mm <Z> :**GBT** (+34C) => **+24C**

Extend to 98mm along Z => **+21C**

GBT now within 10 degrees of wiggle configuration.

Assuming pcb vias: +11C (operation) / +56C (integration)



Material Cost of Foam:

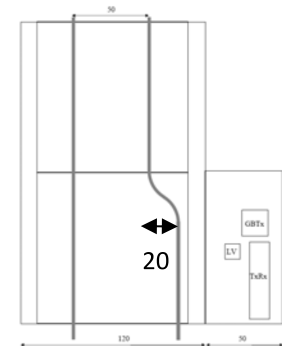
Foam 56 x 98 x 4mm total, ρ = 0.25, X0 = 43g/cm^2: **0.13 cm^2**

cf **Ti pipe wiggle**: 36cm x 2mm id x 0.14mm wall, ρ = 4.51, X0 = 16.2 g/cm^2 : **0.1 cm^2**

SMC boards - !!FR4 ONLY 3 x 10 x 0.16 cm^3, X0 = 16.8cm : **0.6 cm^2**

- conclude no need to worry about foam inserts (use more if helps?).

Additional Strategy: Divert the Cooling Pipe towards the SMC –



Somehow shape pipe (e.g. zig-zag to reduce distance to SMC? Tricky. . .
e.g. Shift pipe 20mm towards SMC => **Further cools GBT by 3C**.
BUT: **Knocks 4C off Runaway Headroom!**

WHY?

- STAVE Cooling philosophy is to distribute the cooling pipes evenly across the sensor. . .
Disturbing this increases thermal resistance R_T (Sensor Heat => Coolant) (above: by 16%).
(A change in R that increases the sensor T (in absence of leakage current) by ΔT reduces the headroom by ~ 3xΔT. Changing R is 3x as dangerous as changing Q, cf straight pipe result).

- Introducing a small meander into the pipe to help cool the SMC (or for other reasons) can seriously harm the runaway headroom: could be done but would involve some TLC and yet more foam ….

Summary

- In absence of the Wiggle”, ~3W EoS(SMC) heat will not seriously degrade runaway performance – at least if the fluid outlet (lower temperature) is on the same side of the stave.
- GBT chip T: Nothing is quite as effective as wiggling the cooling pipe to pass under the chip. . .

. . .but inserting 30W/mK foam into the core can approach it to within ~ 10 degrees . .(+11/+56C)

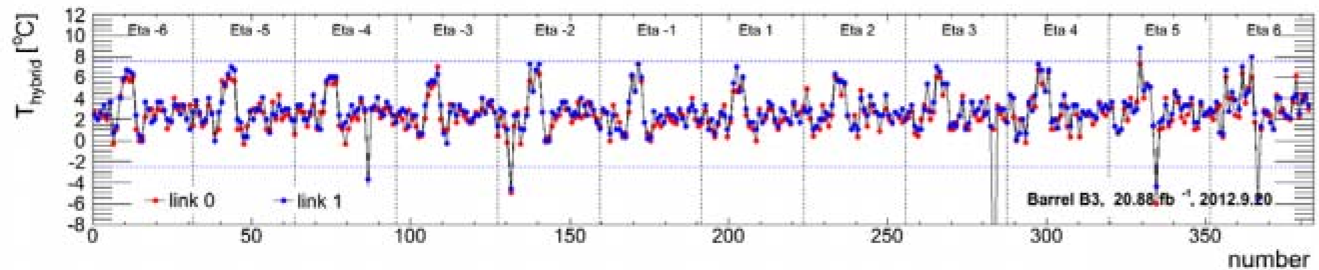
Acceptable? - depends on what is an acceptable chip temperature (assuming model OK!).

<u>It would be helpful to understand better:</u>

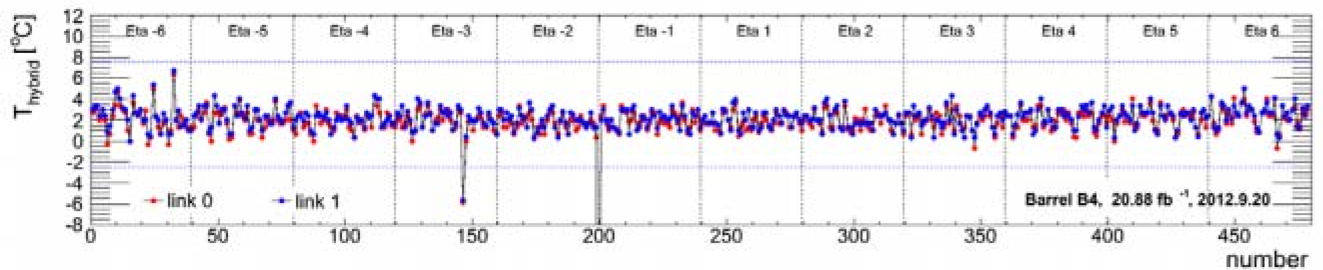
- (trivially) how the hybrids will be placed along Z (symmetrically or not).
- dimensions the SMC card – (problem if chips too far from pipe!).
- what PCB thermal vias are possible.
- packaging / thermal paths of the EoS chips (GBT, GBTLD, GBTLIA, VECSL)
- how efficiently the LV conversion can be done.
- What are the acceptable T ranges for EoS chips: during operation? during integration? (lifetime/ reliability issue !).

BACKUP:
Plots from Steve McMahon of Current SCT temperature:

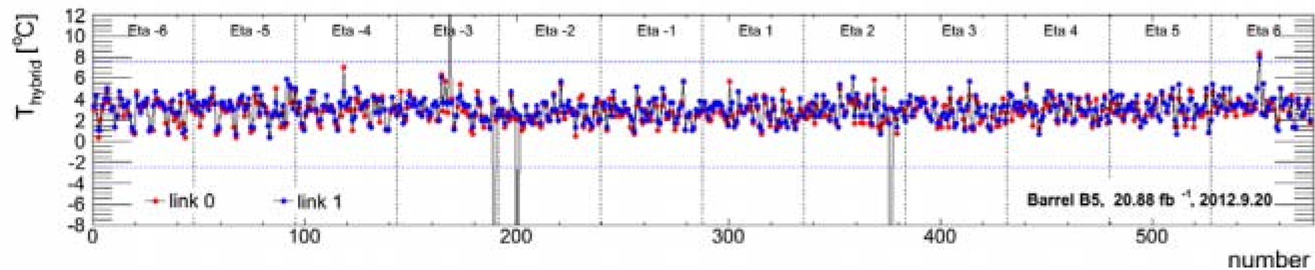
T_{hybrid}



T_{hybrid}

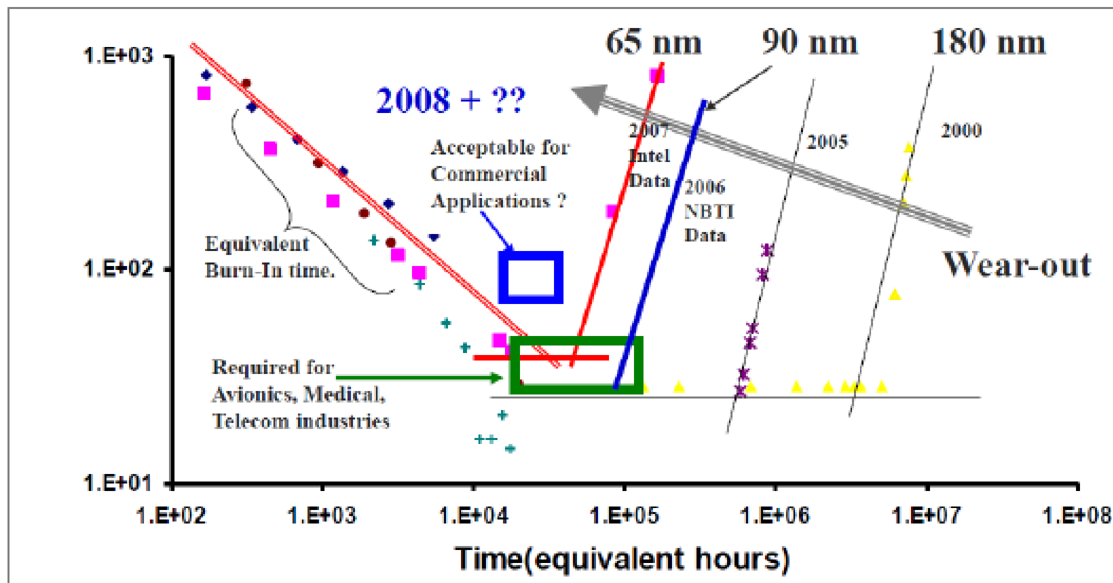


T_{hybrid}



FA Webinar- Cheryl Tulkoff

Failure Rates and The Bathtub Curve



- Field data shows that each new generation of integrated circuits is beginning to wearout sooner than the last
  - Typically misconstrued as pre-mature wearout

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