Pixel DAQ Overview

Andreas Korn
University of Edinburgh

Andreas.Korn@cern.ch

Introduction

- Need to arrive on a solution for larger tests and eventual full scale readout of Pixels/Strips
- Sharing between Pixels/Strips as in the past desirable
- Easy use of existing PixelDAQ
- Discussed with: Matt Warren, Peter Phillips, Craig Buttar
- Slides & pictures stolen from various people (ATCA : Su Dong, Mike Huffer, Martin Kocian, etc)
- Note IBL discussion this Friday: https://indico.cern.ch/conferenceDisplay.py?confId=254325
- Today: overview of what is out there

Readout Options Overview

- Single (few e.g. 4) chip
  - TurboDAQ (no new systems)

    http://physik2.uni-goettingen.de/~jgrosse/TurboDAQ/
  - USBPix

    http://icwiki.physik.uni-bonn.de/twiki/bin/view/Systems/UsbPix
  - SEABAS

    http://rd.kek.jp/project/soi/seabas.html

Readout Options Overview

- Multi module
  - ROD

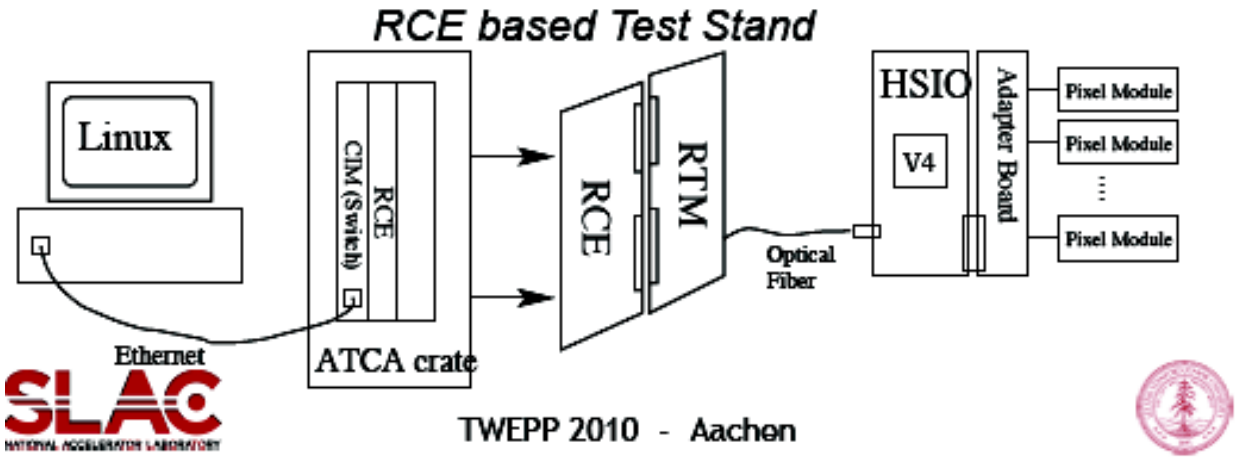
    https://twiki.cern.ch/twiki/bin/view/Main/AtlasSiliconRodGroup
  - IBLROD

    https://indico.cern.ch/getFile.py/access?subContId=0&contribId=0&resId=0
  - ATCA system Gen1 RCE
  - ATCA system Gen3 COB (future)

    https://indico.cern.ch/materialDisplay.py?contribId=168&sessionId=10&ma
  - FELIX (GBL concentrator) based (future)

    https://indico.cern.ch/materialDisplay.py?contribId=115&sessionId=10&ma

Readout Option: ATCA Gen1

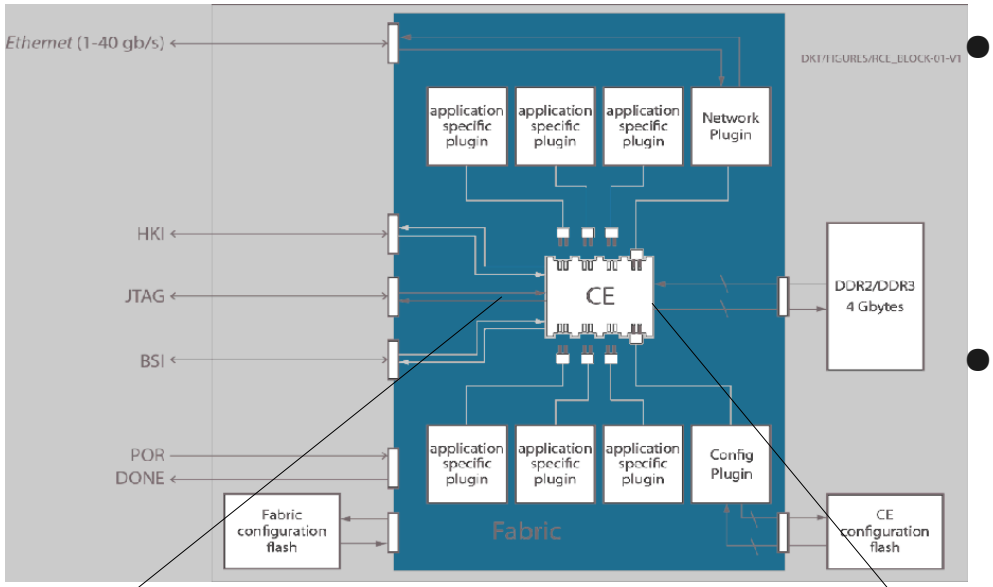


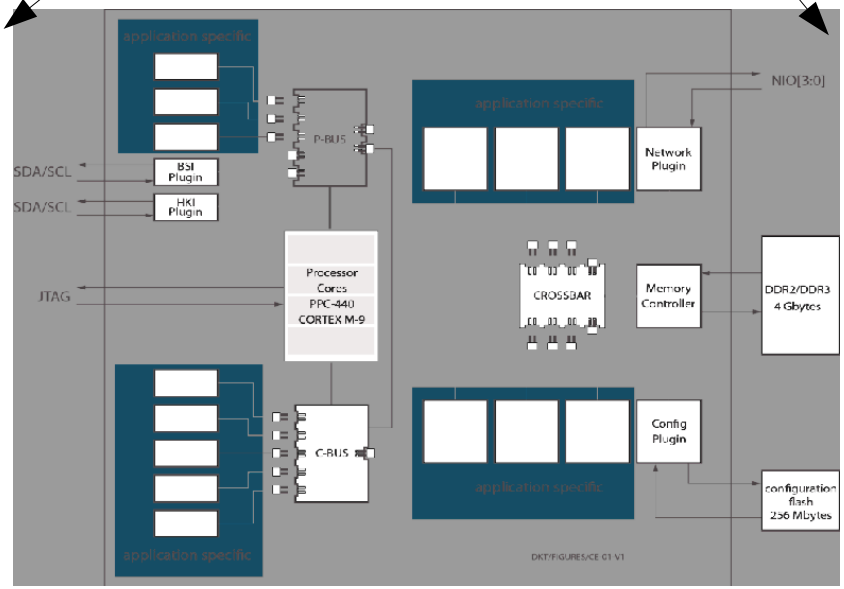
- Flexible system based on SLAC components
- Gen1 deployed in several locations

(SLAC, CERN, Geneva, Glasgow, Liverpool)

- In current configuration upto 8 FEI4 per RCE
- Cost: shelf >2k, RCE ~700, HSIO <2k, CIM

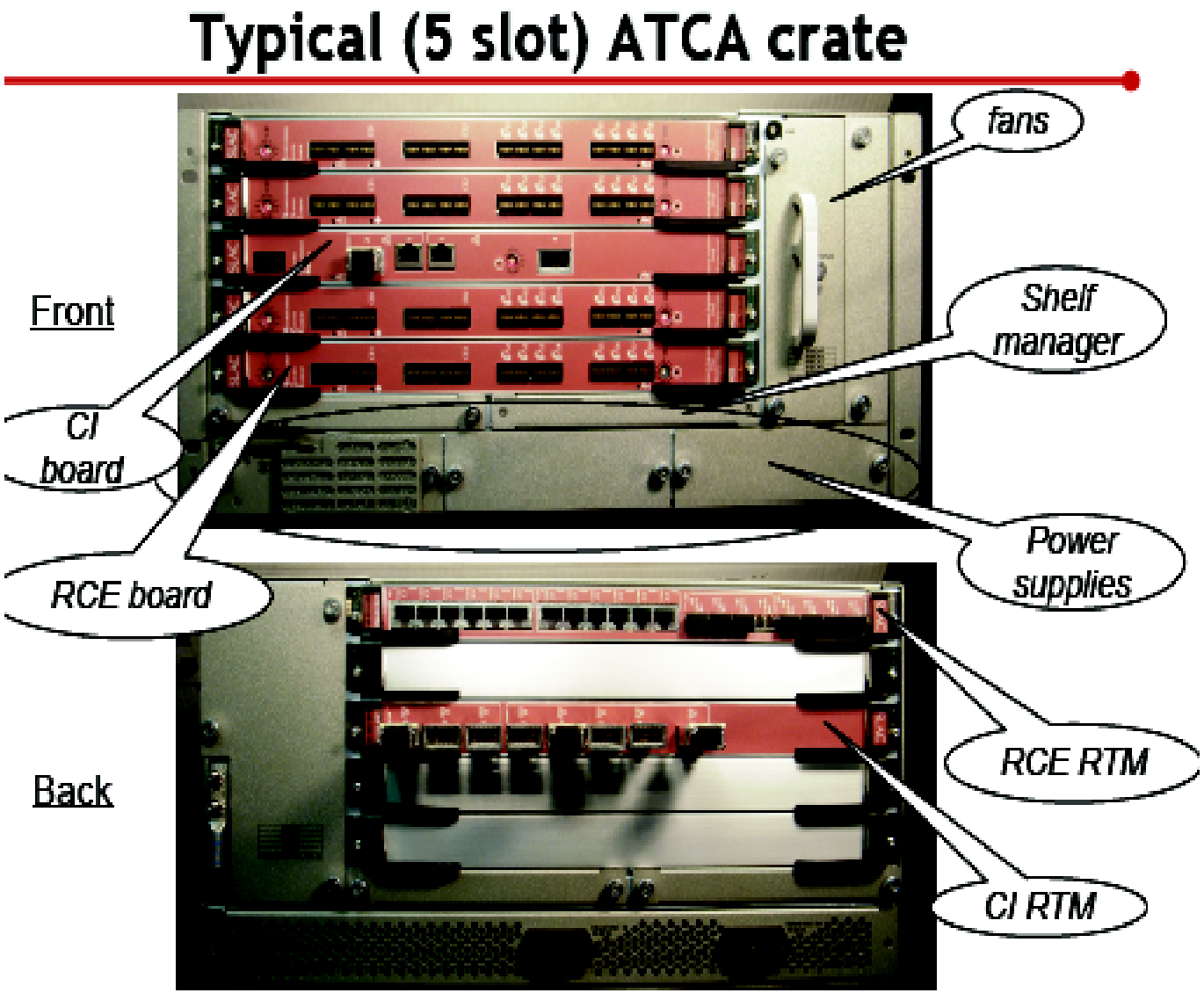
ReadOut Options: ATCA Gen1





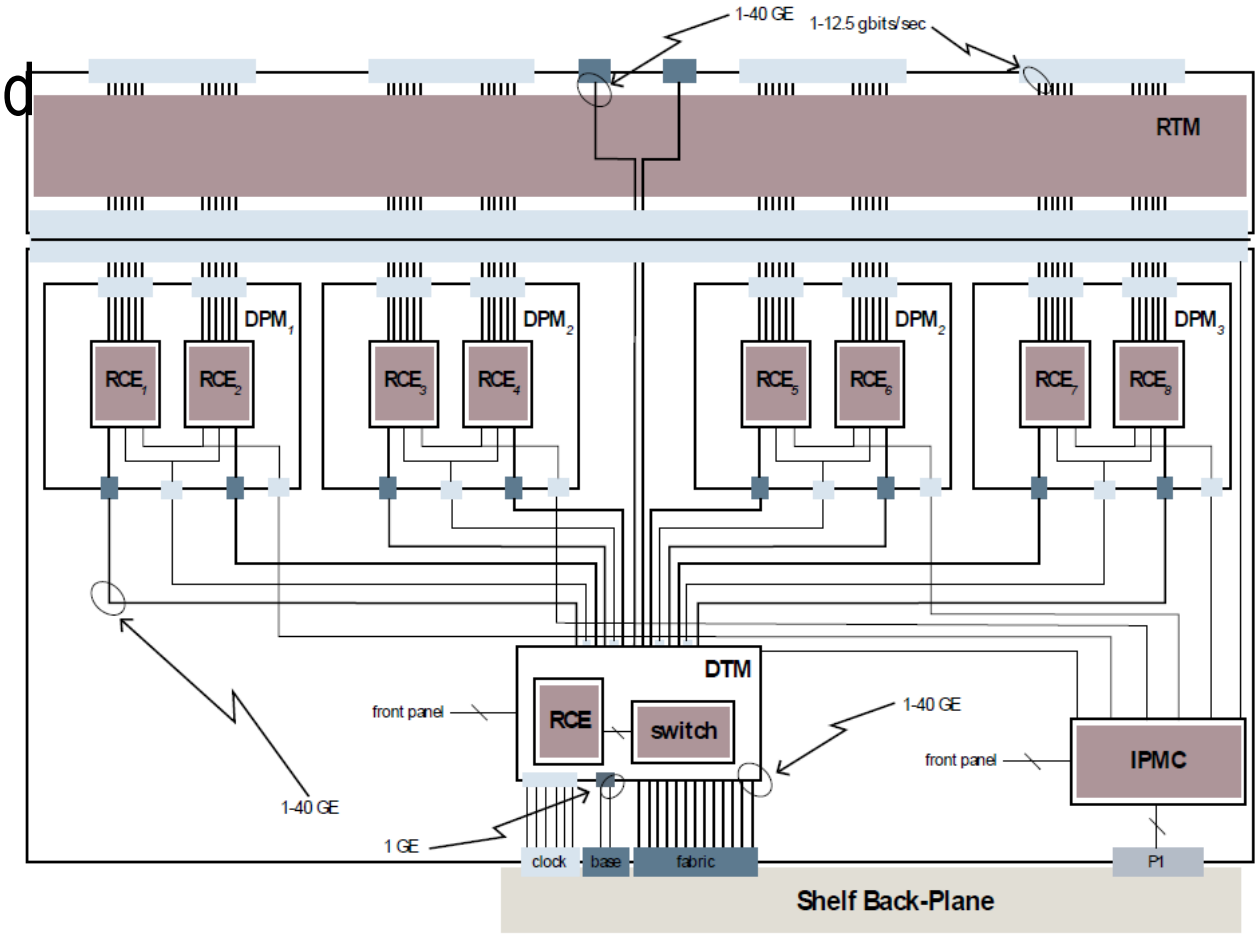
- ATCA
  – Advanced Telecom Computing Architecture
- RTM
  – Rear Transition Module plugs into the back of a crate
- HSIO
  – HighSpeed Input/Output
- RCE
  – Reconfigurable Cluster Element

ATCA: Advanced Telecom Computing Architecture

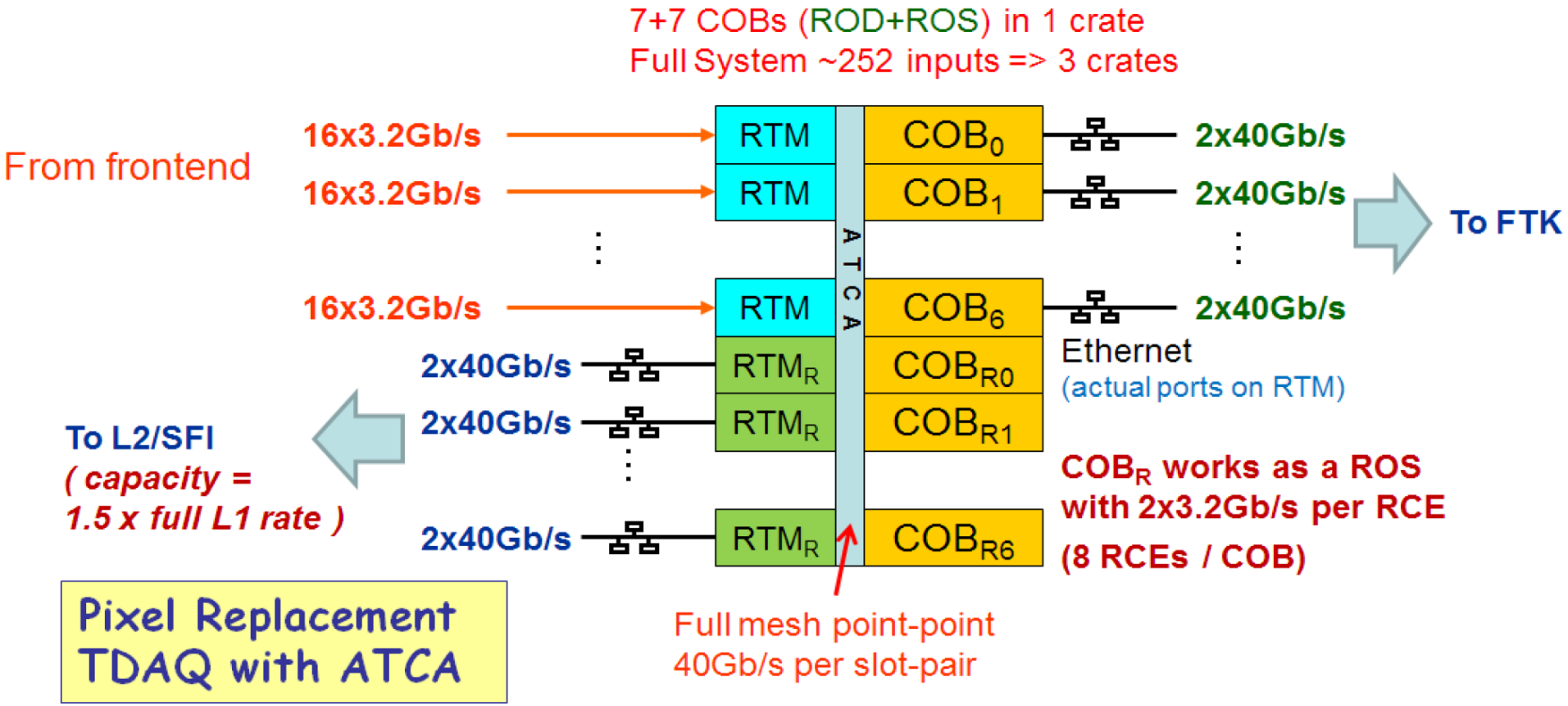


Readout Option: ATCA Gen3

- Gen2 development scrapped
- Cluster on a Board (COB)
- Xilinx Zynq based
- improved performance
- Improved board density
- Some crateless operation
- Timescale: next year?



Readout Option: ATCA Gen3



Conclusions

- Many readout options exist
- For single chips, keep relying on USBPix
- For stave/module setups no longer term solution emerging yet
- For short term ATCA Gen1 solution seems most promising (upgrade to Gen3 seems possible)

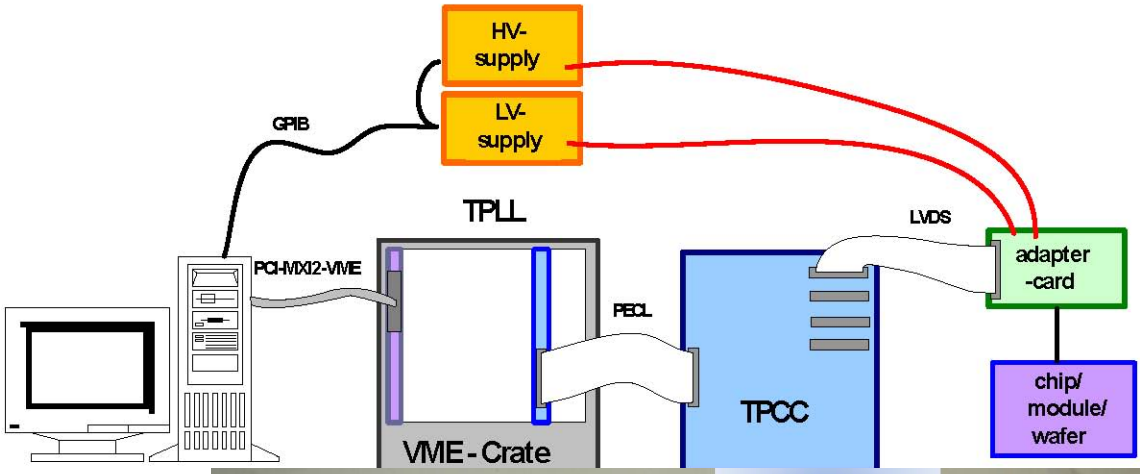
Bonus Slides

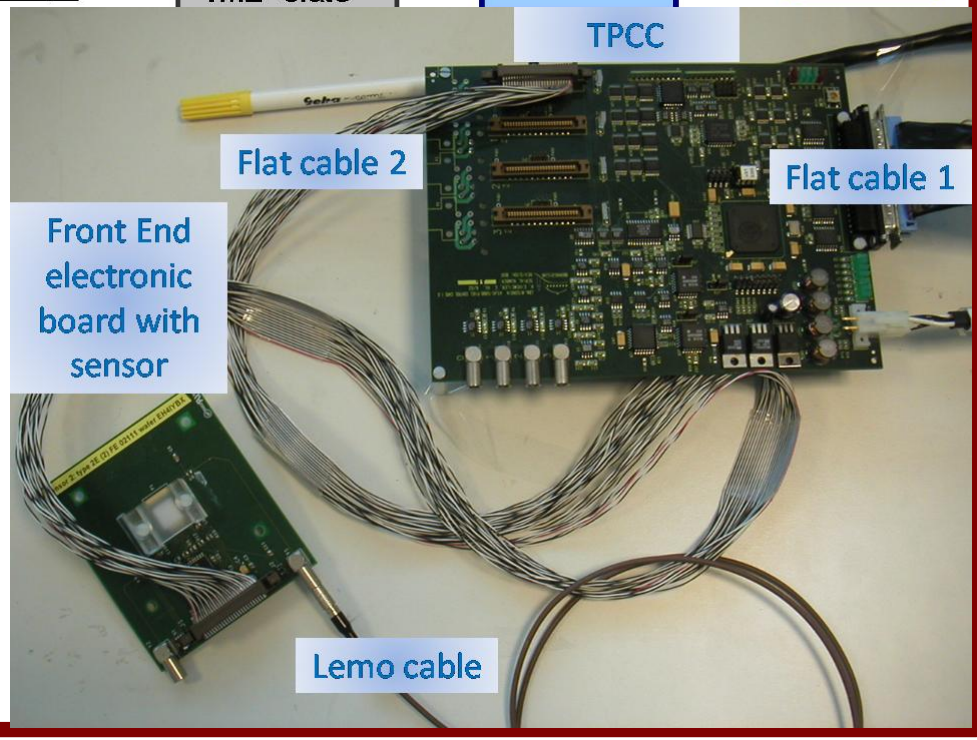
Readout Options Overview

- Single (few) chip
  - TurboDAQ (no new systems)
  - USBPix
  - SEABASS
- Multi module
  - ROD
  - IBLROD
  - ATCA system Gen1 RCE
  - ATCA system Gen3 COB (future)
  - FELIX (GBL concentrator) based (future)

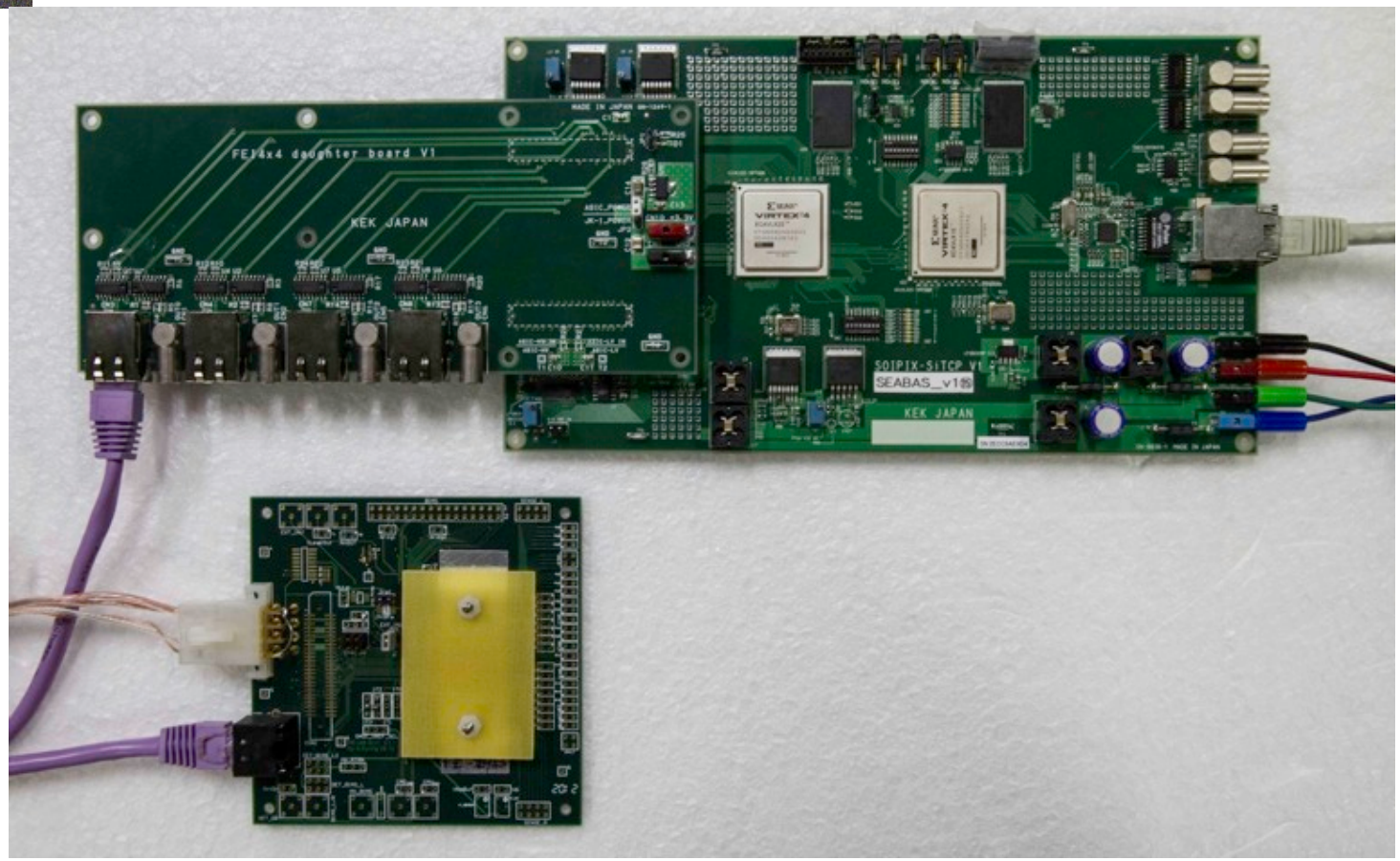
READOUT details: TurboDAQ

- Old legacy system
- Reads one module at a time
- Power & Interlock with SurfBoard
- Still defacto standard for qualifications
- Adaption to FEI4?



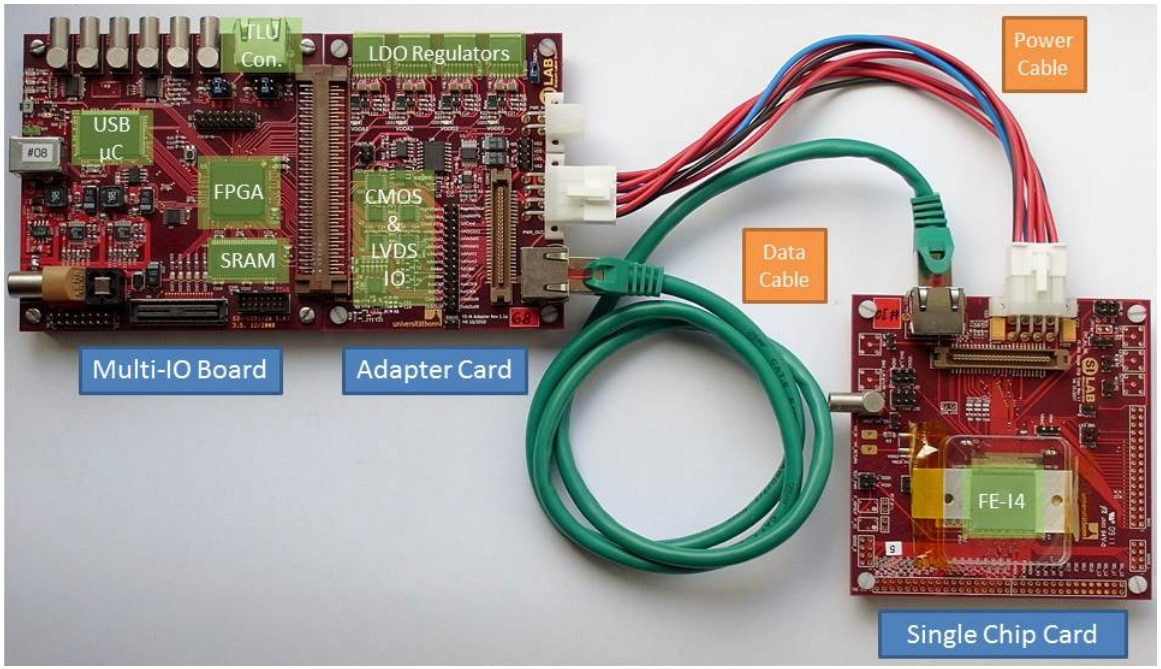


READOUT details: SEABAS



- Based on KEK board, quite flexible
- Handles upto 4 FEI4's, also used with upto 32 strip hybrids
- cost: 2k

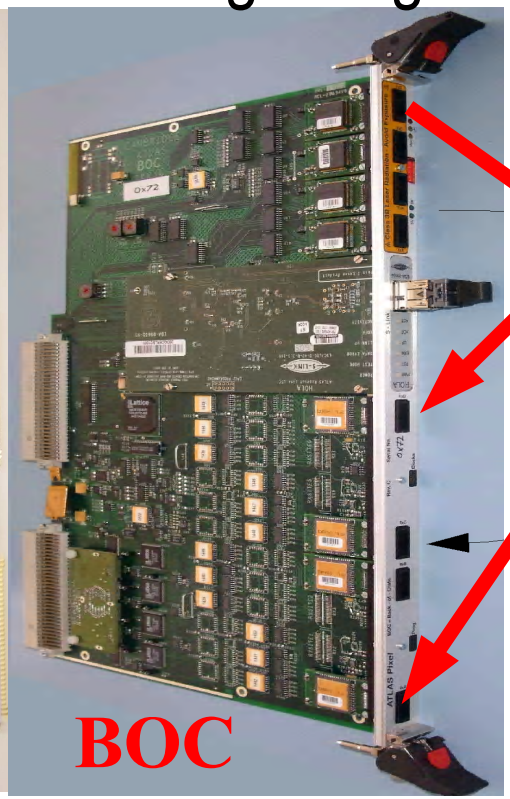
READOUT details: USBPix

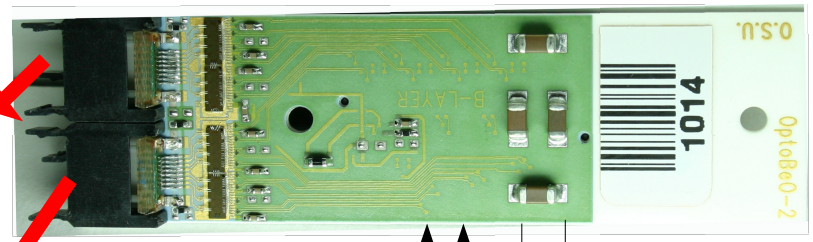


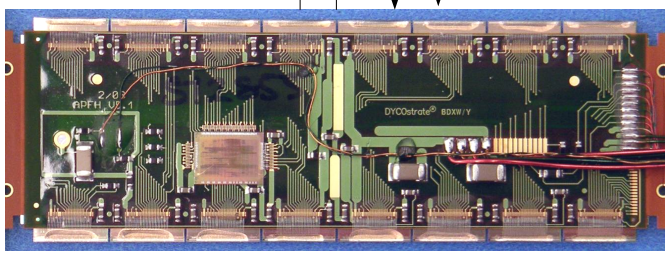
- Quite flexible (FEI3, FEI4, Medipix,)
- In general handles one chip at a time
- Most common FEI4 single chip test setup
- < 1kEuro

Pixel ReadOut: ROD

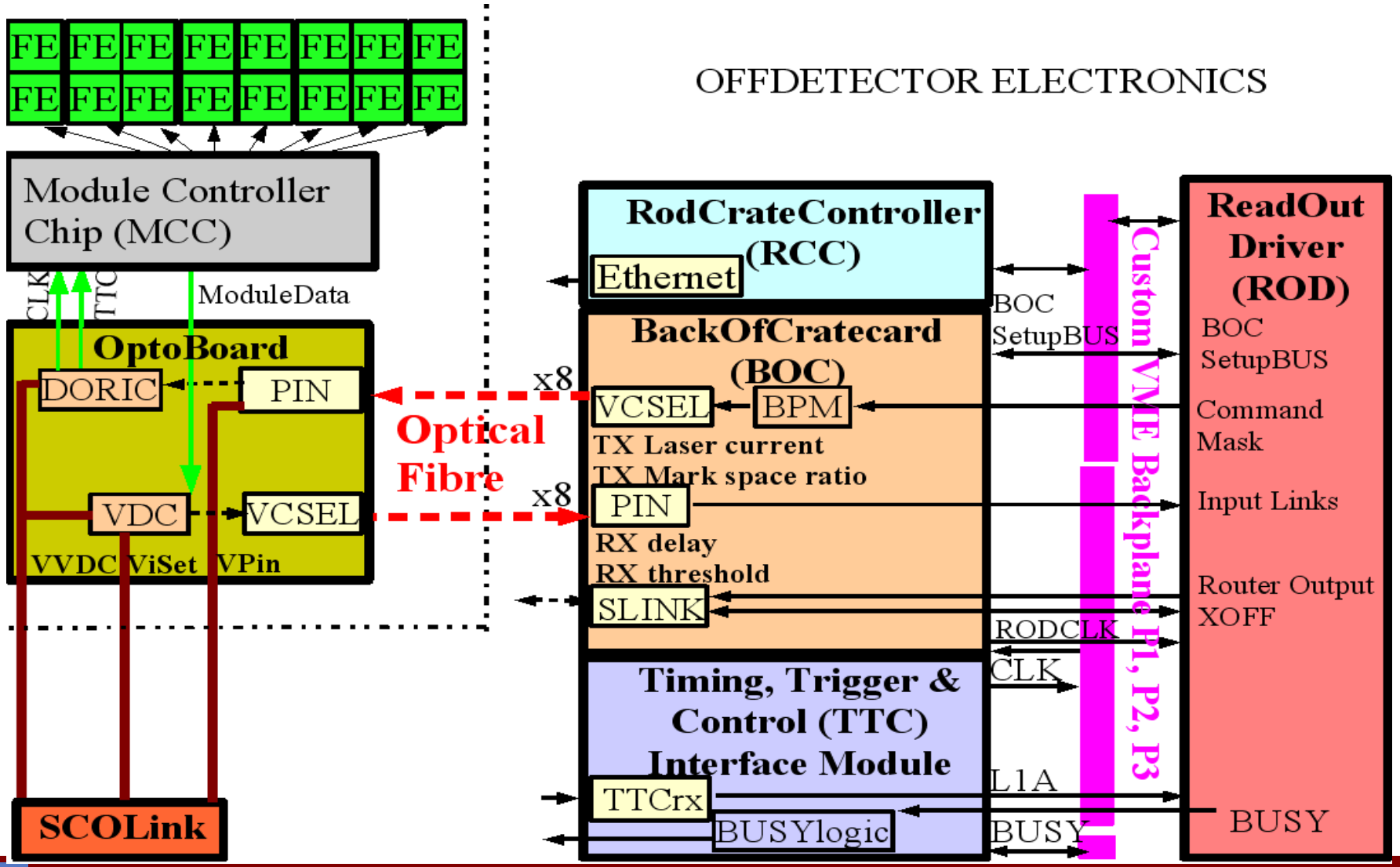
- upto 28 Modules can send data with 40(L2), 80(L1, Disk) or 160 Mbit(B)
- 4 LVDS connections to Module: Clock, DataIn, 2 x DataOut
- optoBoard services 6/7 modules, converts electrical to optical
- BackOfCrate card encodes clock/data, decodes in 40MHz streams
- ReadOutDrive with 4+1 DigitalSignalProcessors and 1GB RAM



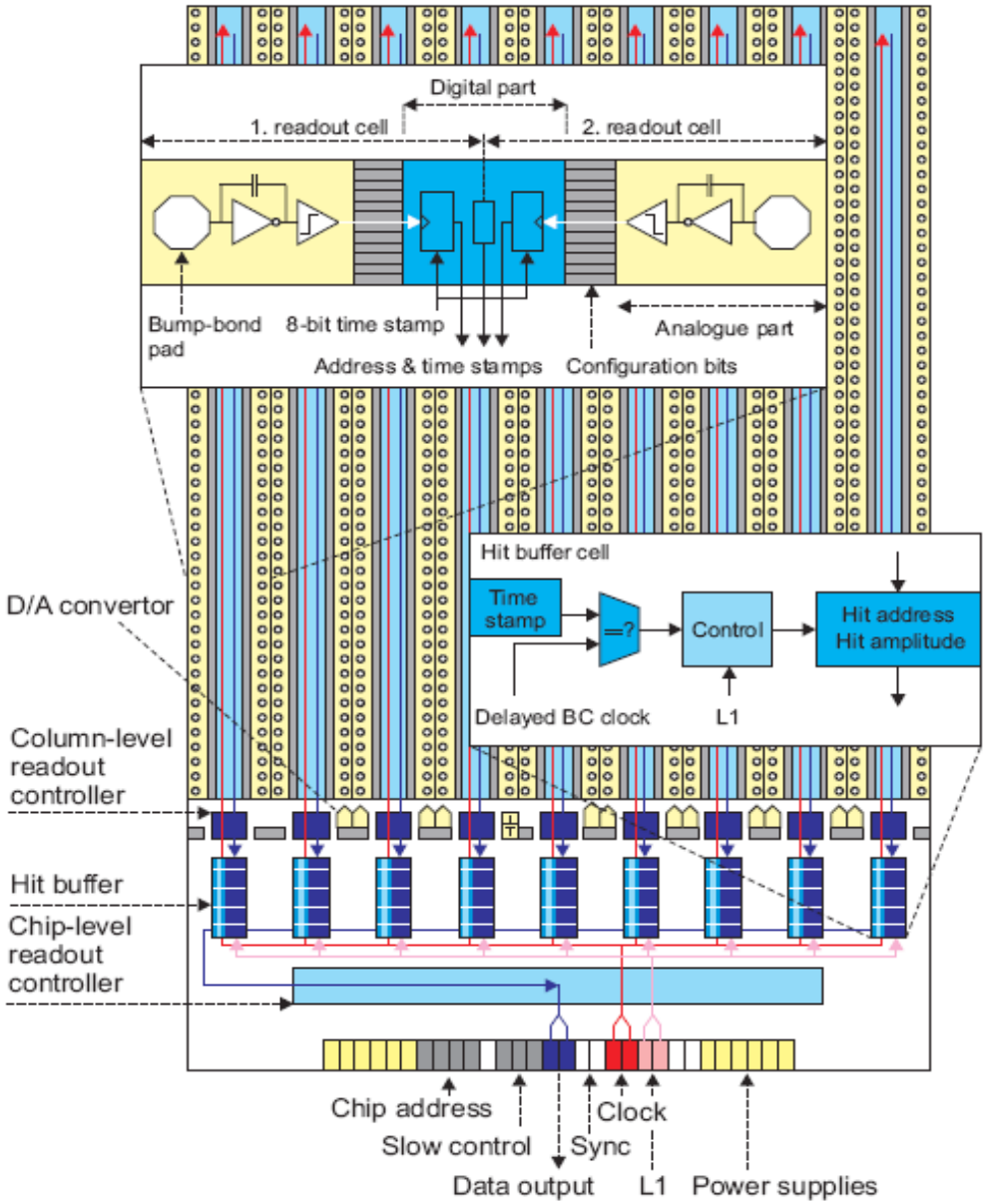


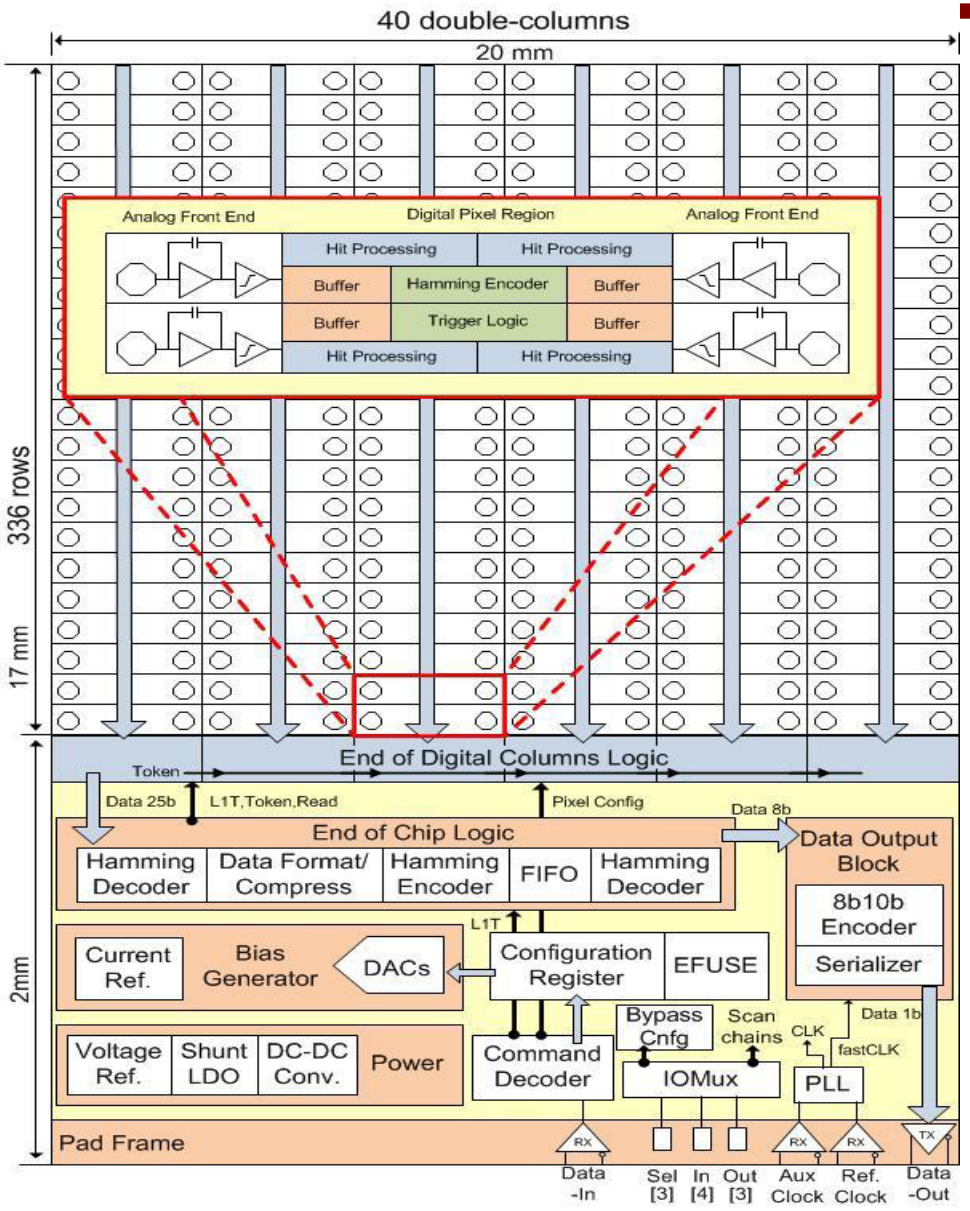


PixReadOut: ROD

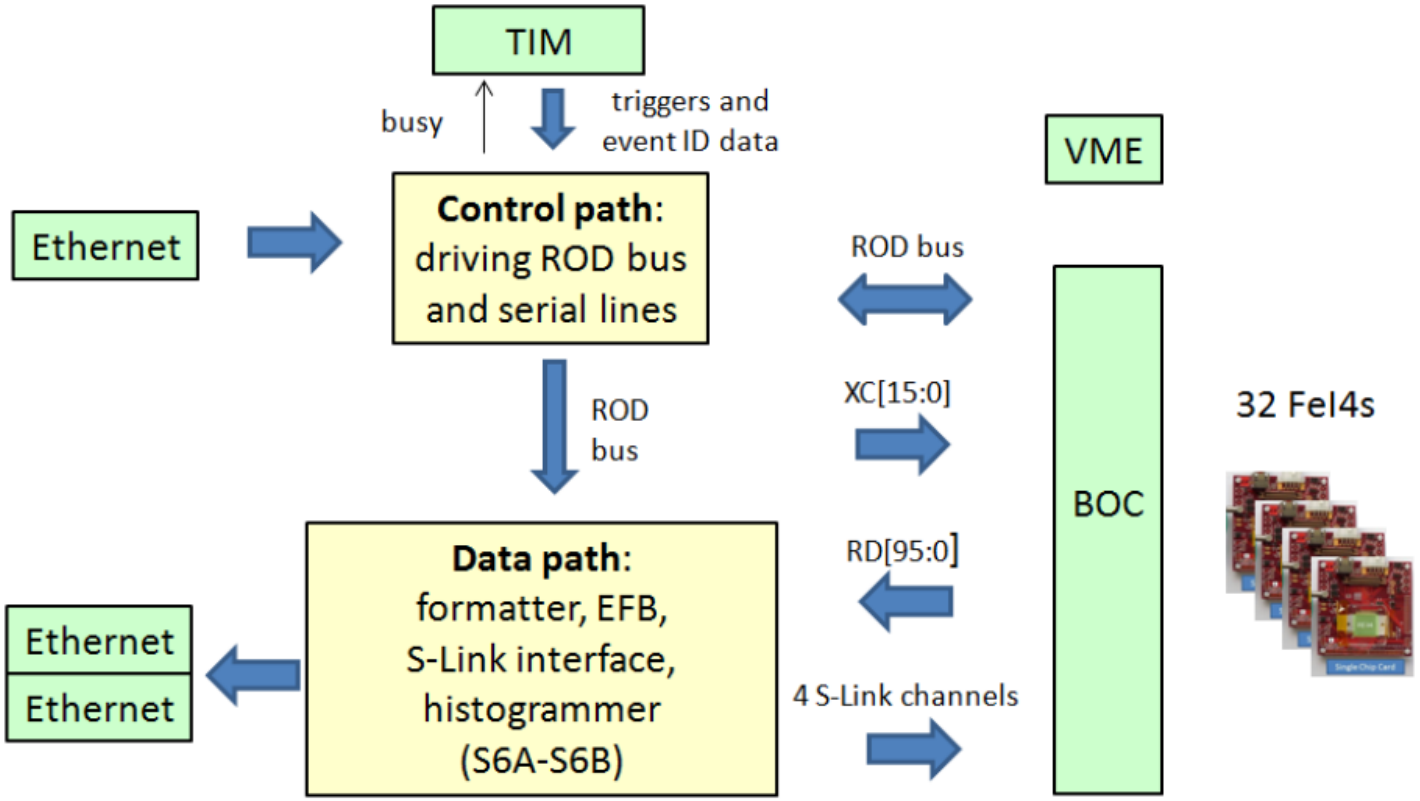


FEI3 vs FEI4


Digital part
1. readout cell
2. readout cell
Bump-bond pad
8-bit time stamp
Address & time stamps
Configuration bits
Analogue part
Hit buffer cell
Time stamp
=?
Control
Hit address
Hit amplitude
Delayed BC clock
L1
D/A convertor
Column-level readout controller
Hit buffer
Chip-level readout controller
Chip address
Slow control
Sync
Clock
Data output
L1
Power supplies

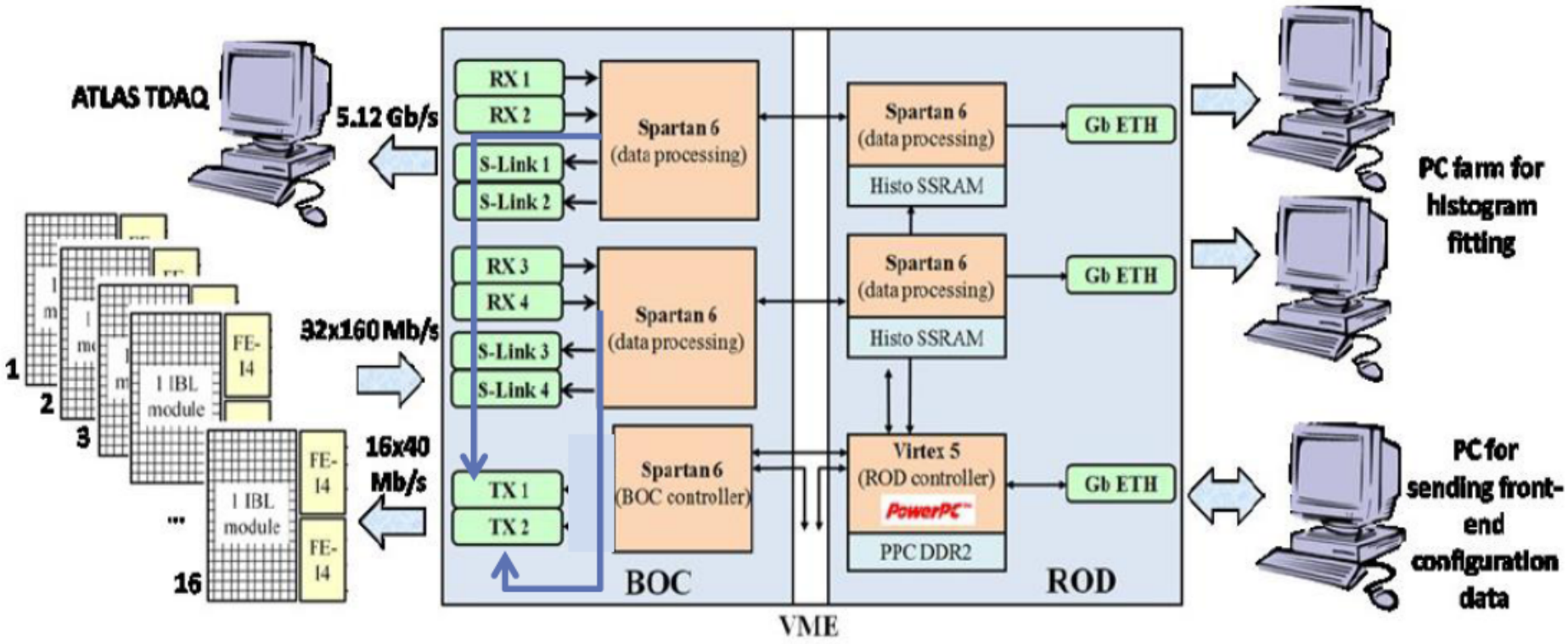

40 double-columns
20 mm
336 rows
17 mm
2mm
Analog Front End
Digital Pixel Region
Analog Front End
Hit Processing
Hit Processing
Buffer
Hamming Encoder
Buffer
Buffer
Trigger Logic
Buffer
Hit Processing
Hit Processing
End of Digital Columns Logic
Token
Data 25b
L1T,Token,Read
Pixel Config
Data 8b
End of Chip Logic
Hamming Decoder
Data Format/ Compress
Hamming Encoder
FIFO
Hamming Decoder
Data Output Block
8b10b Encoder
Serializer
L1T
Current Ref.
Bias Generator
DACs
Configuration Register
EFUSE
Bypass Cnfg
Scan chains
CLK
Data 1b
fastCLK
Voltage Ref.
Shunt LDO
DC-DC Conv.
Power
Command Decoder
IOMux
PLL
Pad Frame
RX
TX
Data -In
Sel [3]
In [4]
Out [3]
Aux Clock
Ref. Clock
Data -Out

PixReadOut: IBLROD



- Updated ROD architecture
- Better debugging and calibration dataflow
- Removed bottlenecks: S-Link & now upto 32 FEI4 160 Mb.s links
- Tests & commissioning ongoing

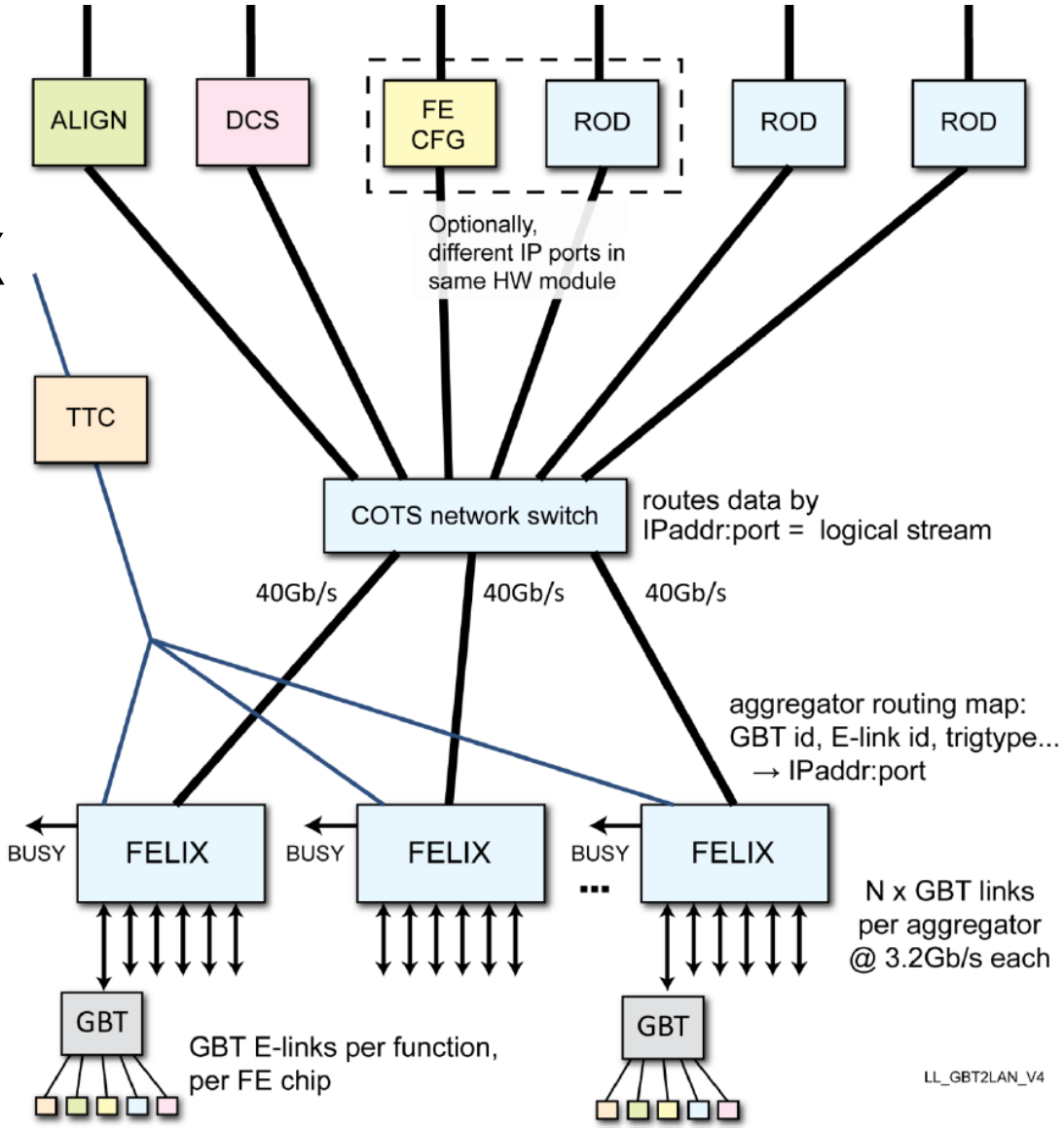
PixReadOut: IBLROD



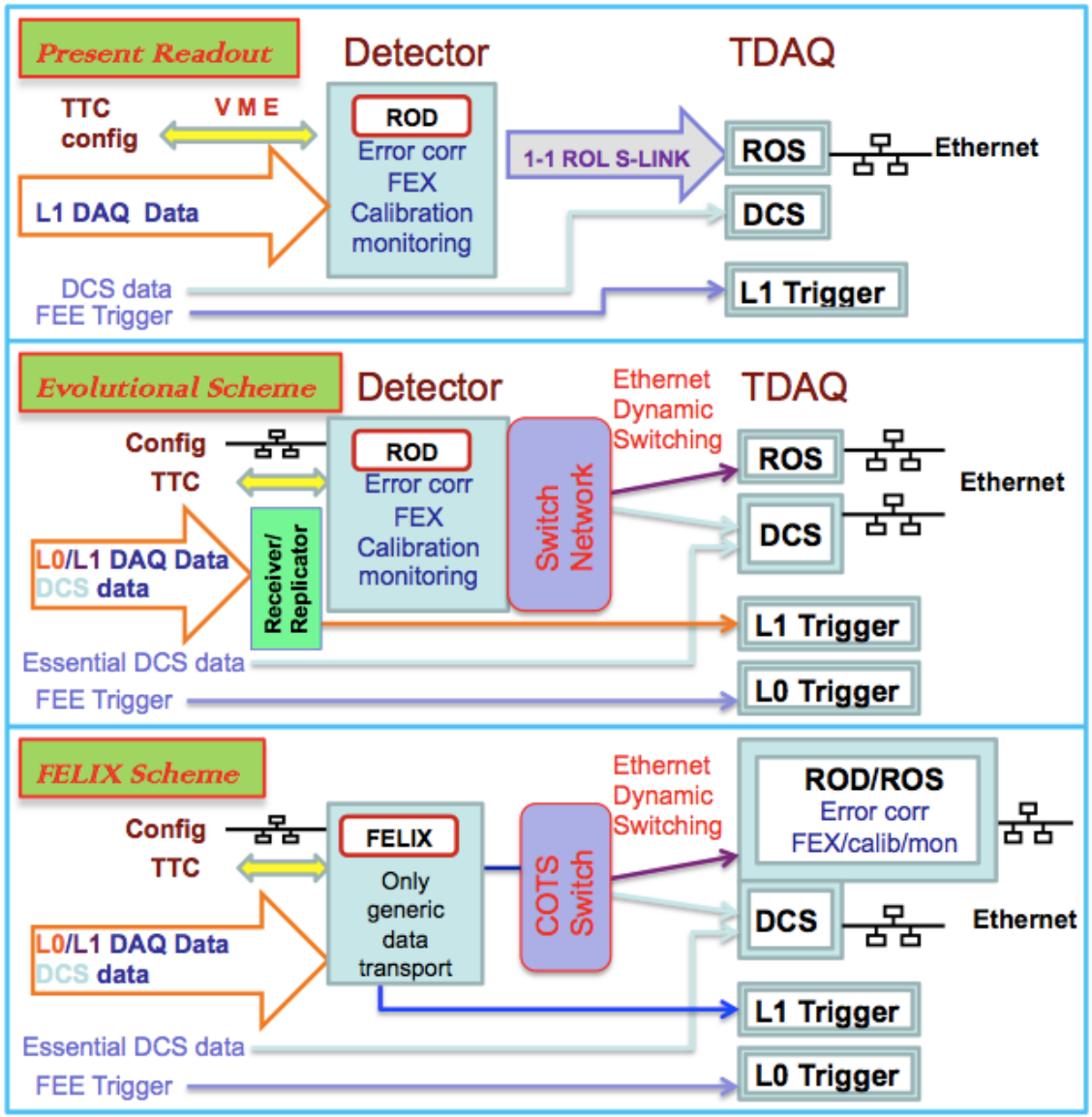
- Updated ROD architecture
- Better debugging and calibration dataflow
- Removed bottlenecks: S-Link & now upto 32 FEI4 160 Mb.s links
- Tests & commissioning ongoing

ReadOut Option: FELIX

- Interfacing to Front End LinX
- Any DAQ done via ethernet on PCs
- So far vaporware
- Could be interesting long term

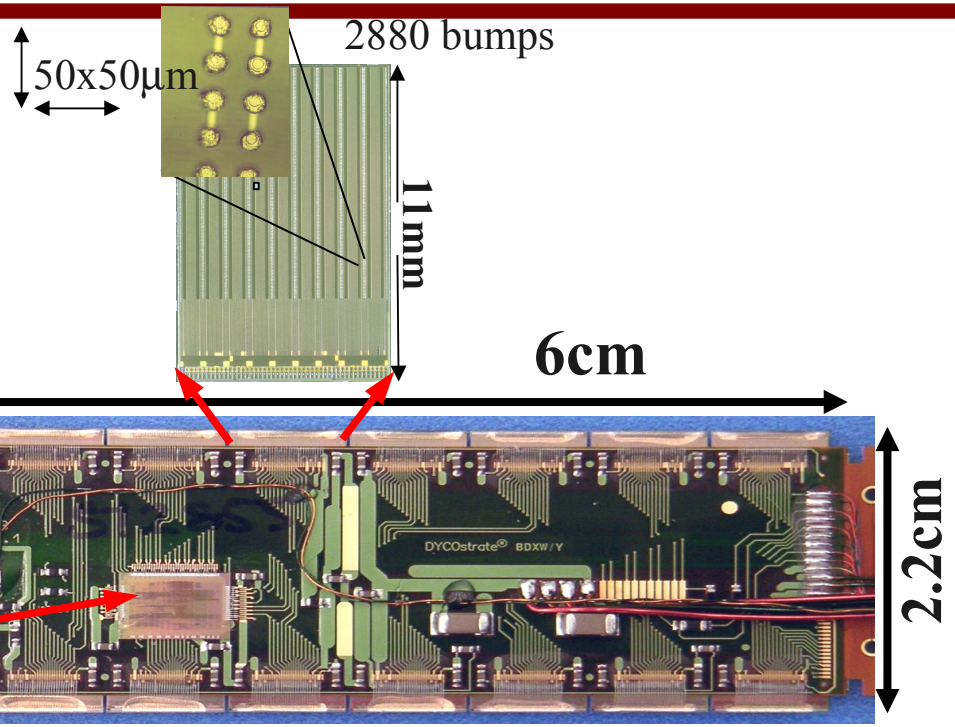


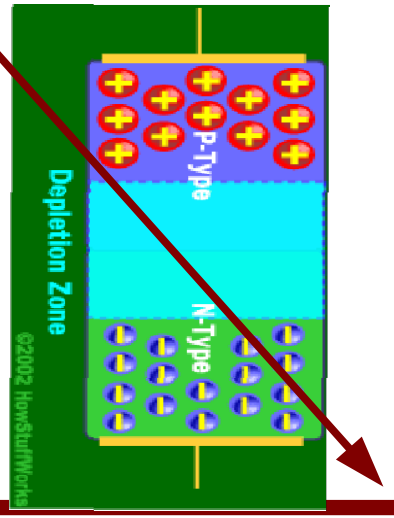
ReadOut Option: comparison

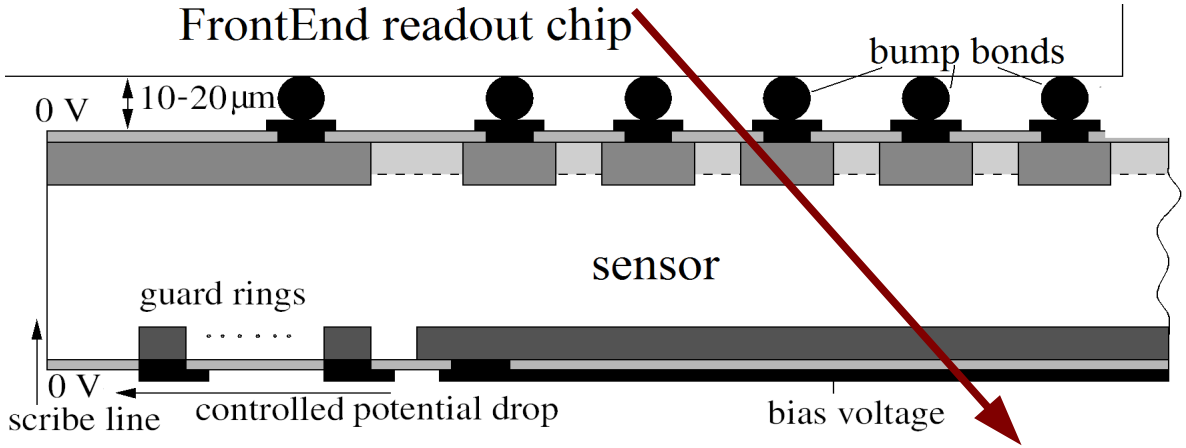


Current Pixel Module/Silicon Sensor

Good spatial resolution
→ 50µm x 400µm Pixels
Fast readout (25ns beam crossing)
Radiation hardness
→ Hybrid chip technology
0.25µm CMOS FrontEnd
1 sensor bump bonded
to 16 FrontEnd chips
which are connected to a
ModuleControllerChip

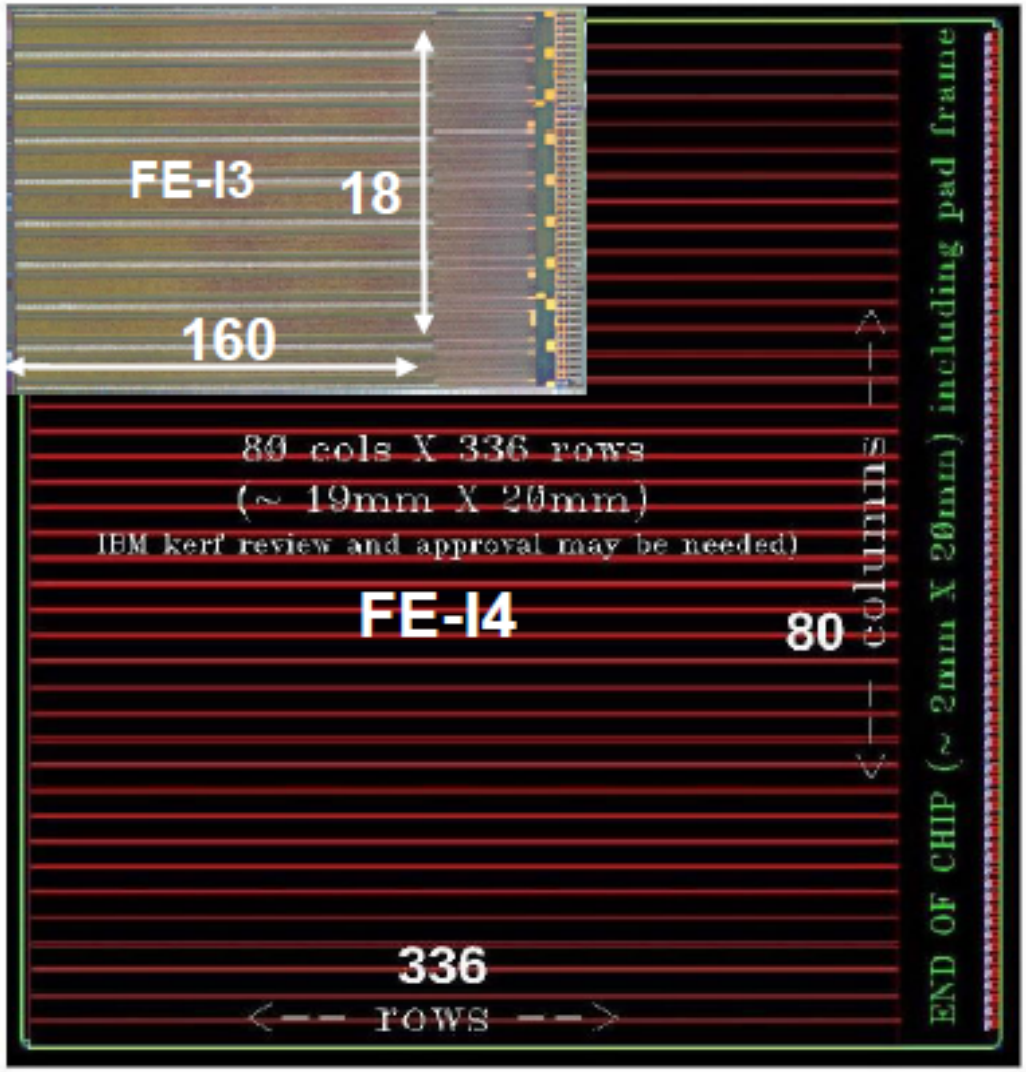




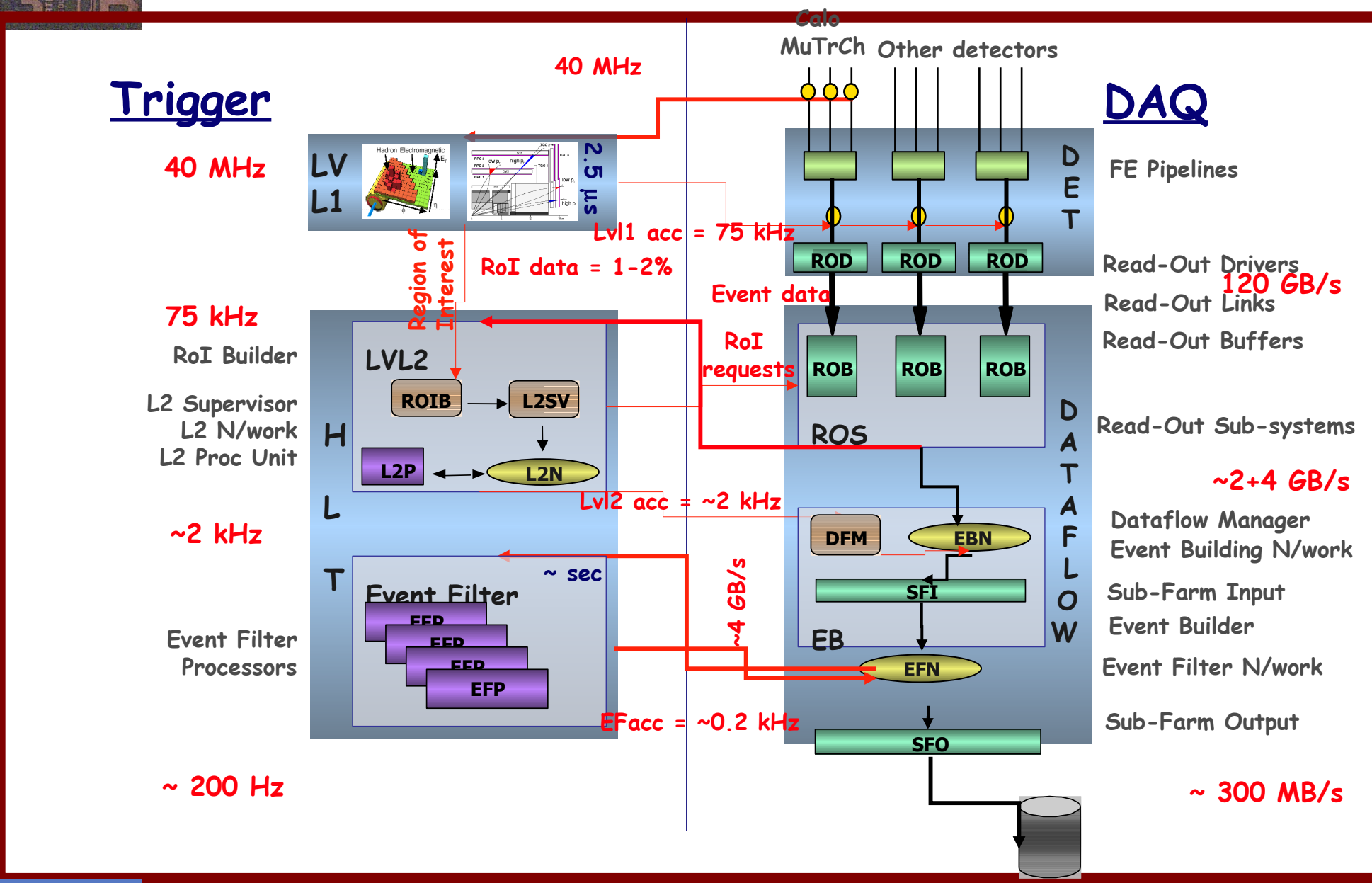


New Pixel FrontEnd Chip FE-I4

- Much larger chip area
  → fewer chips cover a module
- Better resolution:
  → 50µm x 250µm Pixels
  (25µm x 150µm in preparation)
- Can now handle higher occupancy

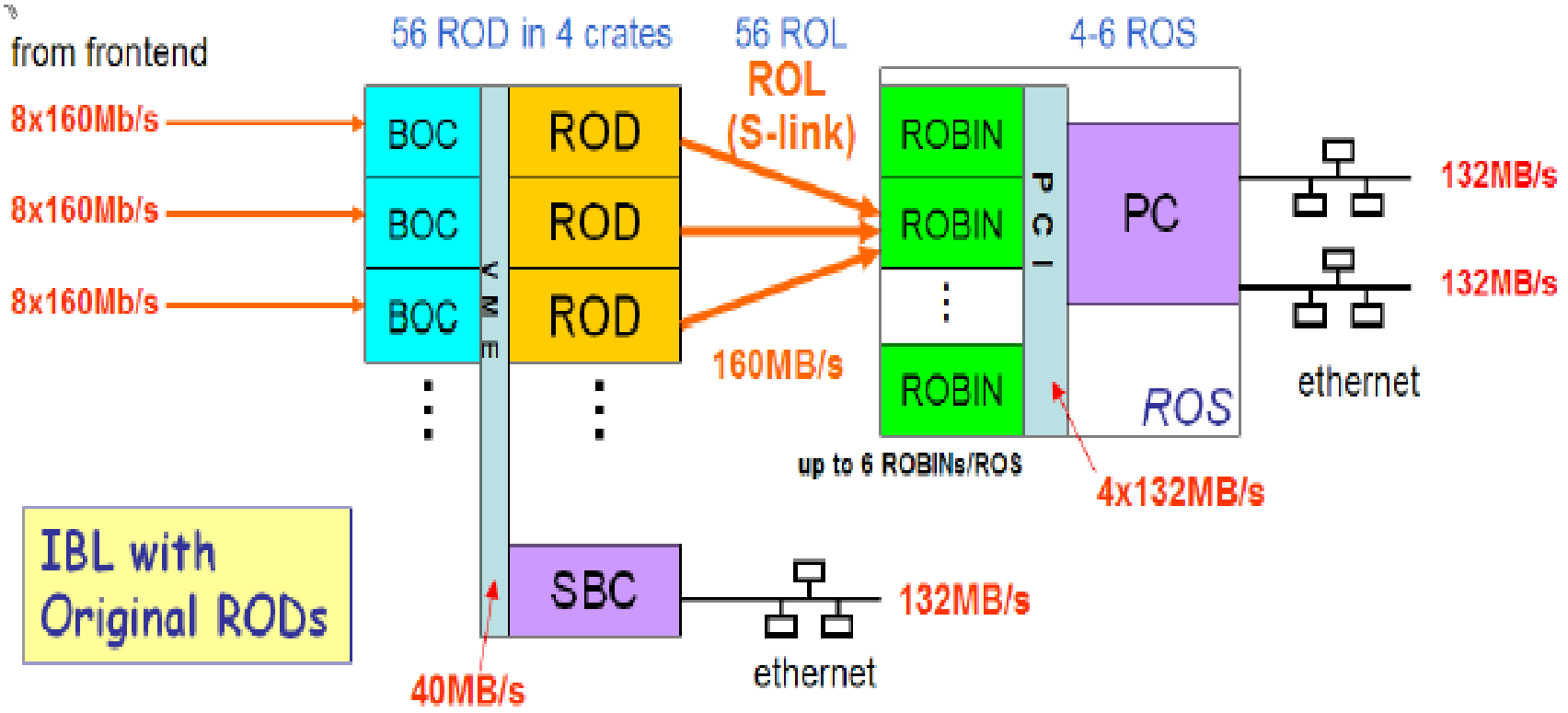


Current ATLAS Trigger/DAQ



READOUT details

Example case: IBL readout with old VME RODs:



Acronyms

- FE-I3 – current Pixel front end chip
- FE-I4 – Pixel front end chip for IBL
- ABC chip – current silicon strip readout chip
- ABC130N- upgraded strip readout chip
- MCC -Module Controller Chip to readout 16 FEI3
- Optoboard -
- HCC – Hybrid Controller Chip
- ROD - Read Out Drive
- TTC- Trigger Timing and Control

Acronyms

- TIM – TTC Interface Module – send clock + trigger
- GBT – Gigabit Transceiver
- S-Link – sends data from ROD to ROS
- ROB – ReadOut Buffer
- ROBIN – physical card housing ROBs in the ROS
- ROL – ReadOut Link
- ROS – Read Out System
- TX/RX plugin – optical transmission/receiving pluging on the BOC
-

Acronyms

- ATCA – Advanced Telecom Computing Architecture
- RTM – Rear Transition Module plugs into the back of an ATCA crate
- HSIO – HighSpeed Input/Output
- TOT – Time Over Threshold
- TDAC – Threshold DAC
- FDAC – Feedback DAC
- SBC -Single Board Computer, controls the DAQ crate, also RCC (ROD Crate Controller)
- FTK – Fast Tracker (L)

Acronyms

- BCR – Bunch Counter Reset
- ECR – Event Counter Reset
- L1A – Level 1 Trigger Accept Signal
- LVDS – Low Voltage Differential Signal