**Fabrication, Assembly and QA/QC for PixFlex Hybrids**

**Version 0.1**

**Abstract**

The implementation of quality assurance (QA) and quality control (QC) procedures is an important part of the development of an electronic design.This document covers the approach for fabrication, assembly and cleanliness of the PixFlex Hybrid giving a detailed insight on the QA and QC tests to be performed.

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# Introduction

The flex hybrid will be a flexible PCB made on kapton that will sit on the rear (unpatterned) face of the Silicon sensor. It will serve several purposes:

* Route clock and control, LV and HV, and data to and from the FE-ASICs.
* MUX (data multiplex) chip will sit on the hybrid and multiplex data from 4 FE-ASICs.
* The Pixel Serial Powering and Protection (PSPP) chip will sit on the hybrid and control the SP of the FE-ASICs LV.

Further details of the design are given in the Flex Specification document (to be written). The detailed design of the flex is given Flex design document (to be written)..

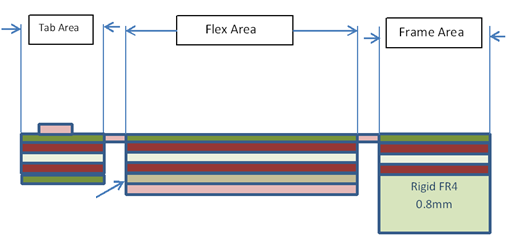
These Flex circuits will be fabricated in Industry using industrial approved standards and meeting our design requirements.

The assembly of the Flex circuits will also be done in Industry where the Flex will be populated with the passive components.

Further assembly will be done in house. The MUX (data multiplex) and PSPP (pixel serial power protection) chip are attached to the flex with glue and wirebonded for electrical connection in house. The flex is attached to the backside of the sensor on the pixel assembly (Silicon sensor bump bonded to the FE chip), see module assembly document for details. This is called a module. The electrical connection of flex to pixel assembly is performed in house with wirebonds. Final module test take place as explained in the Module test document.

# Design overview

The flex concept is based on a minimal number of copper on kapton layers to minimize material. This is a double-sided, copper-clad laminate and an all polyimide (AP) composite of polyimide film bonded to copper foil. The flex build is conceptually given in Figure 1.



Stiffener LF0110

Soldermask EFP14

AP8515 Cu 9um/18um, Dielectric 25um

Soldermask EFP14

25um Acrylic Glue

25um Kapton coverlay

Figure

Cross section of the Pix Flex Build

The top solder mask is required for the soldering of components and is required to be flexible. The soldermask used is Green Flexible Soldermask EFP140. The 18um (or 9um) top copper layer on kapton is used to route all the signals on the body of the flex. The backside copper layer is used as a stress relief layer to obtain a flatter build. This is covered with a coverlay (25um coverlay with 25um acrylic glue).The glue will be replaced with Espanex (modified polyamide) adhesive as acrylic glue is not radiation hard.

The interconnect of the flex to the ring tape is provided by a tab with a connector on the backside. The tab area with connector is selectively solder masked to ease the soldering and avoid solder bridging.

The flex has vias only on the tab area that route the signals from the flex front side to the connector on the back side. These vias are selectively plated to avoid access copper plating on the rest of the flex area.

The flex is held inside a frame for handling. The frame also provides accurate fiducials and cut holes for module construction and stiffness to hold the flex flat. The frame is either the same build as the body of the flex or has an addition 0.8mm thick FR4 laminate on the backside for additional mechanical support.

# Fabrication and Assembly

Fabrication and assembly of passive components on the Flex is planned at ZOT Engineering Edinburgh.

However this is subject to final formal tender.

Assembled flex circuits will be shipped to the respective institutes.

# Cleaning of PCBs at Industry

The flex is cleaned in two tanks. The cleaning chemical Vigon N600 is used in the first tank (NC25-PCB Cleaning tank) then the boards are rinsed with DI water in the second tank. The PCB’s are then hot air dried.

## Minimum Cleaning required for PCB’s

The steps below state the stages in the fabrication process where cleaning would be required to achieve boards with the least contamination. All these tests will be performed at industry.

### QC for Cleanliness of PCBs

The cleaning steps are listed below. After each step IPC-CH-65A will be followed to confirm cleanliness.

#### Cleaning of Bare PCBs

* + Immediately before the application of soldermask.
  + Immediately after the application of any solderability plating.

eg. HASL, ENIG, Immersion Tin, Immersion Silver.

* + A clean after plating.

The following are some of the IPC test methods/standards that are followed to achieve cleanliness of bare PCBs-

* IPC-5701 –User’s Guide for Cleanliness of Unpopulated Printed Boards.

This document defines the recommended general requirements for the

cleanliness of unpopulated single, double-sided or multilayer printed boards.

* IPC-TM-650 - 2.3.25.1 - Ionic Cleanliness Testing of Bare PCBs.
* IPC-6013 - Qualification and Performance Specification for Flex boards.

#### Cleaning of Populated PCBs

* + A final clean after SMD component population.

The following are test methods/standards that are followed to achieve cleanliness of assembled PCBs-

* IPC-A-610D- Has a section that defines acceptability requirements for cleanliness of assemblies.
* IPC-CH-65A has further Guidelines for Cleaning of Printed Boards and Assemblies.

The test methods stated below are performed on bare PCBs as well as assembled PCBs.

IPC-TM-650 Method 2.3.28A (measure ionic contamination on PCB) specifies the process to measure the ionic contamination on PCBs after they are cleaned. This measures the level of extractable ionic contamination on the surface of printed boards and printed board assemblies by ion chromatography. The resistivity of the final rinsed DI water is measured to ensure that it meets the specifications.

IPC TM-650- 2.3.38 Surface Organic Contaminant Detection Test specifies the procedure to test for organic contamination on the PCB.

### QA for Cleanliness of PCBs

A test coupon, **Test Coupon-1**(design explained below)will be designed to perform accelerated aging. The temperature and RH will be raised to a specified value to prove that there is no degradation of the inter-trace isolation.

IPC-TM-650 -2.6.14.1- Electrochemical Migration Resistance Test specifies the test procedures to carry out this test.

A temperature/humidity chamber capable of producing an environment of 40°C ± 2°C, 93% ± 2% RH ; 65°C ± 2°C , 88.5% ± 3.5% RH, or 85°C ± 2°C, 88.5% ± 3.5% RH and allowing test boards to be electrically biased and measured without being opened under these temperature and humidity conditions will be required for this test. The temperature and humidity value for our system under test has to be chosen.

This test needs to be performed on both the bare and assembled PCBs.

# PCB Packaging and Shipping

The assembled PCBs will be handled with lint free gloves once the assembly process is complete till the time they are packed for shipment.

The PCB will be shipped in clean sealed bags to the institute; once opened the PCBs will be stored in an N2 cabinet. At the institute the PCB will only be handled with lint free gloves to maintain the cleanliness of the PCB as shipped. No further cleaning of the PCB will be required at the institute.

# QC (Quality Check) in Industry

QC checks needs to be done on every single PCB in production.

## Post Fabrication

* 100% Net List Test: Check of every "node" on every net on the board.
  + **Flying Probe Testing**: Using the flying probe test sequence to cover all areas of the board including fine pitch and high density points. While doing so we need to be sure that the probes do not damage the wire bond pads.
* Opens Test: Check to make sure there is current flow from one "node" to the next for every net on the board, again by measuring the resistance of the conductor.
* Shorts Test: Check to make sure that NO current flows between separate nets by measuring the resistance between them.

The voltage applied and the resistance tolerance for the open and short test values have to be checked from the industry.

* High Voltage Test: Refers to high voltage potential testing to check for high resistance continuity or leakage between ground and power planes and traces.

High voltage test is designed to validate the insulation between the detector HV trace and planes and all other metal traces.

Spacing between conductors can be calculated as explained in IPC 2221A document (General Standards on Printed Board design).

We will operate at 750V and test for 1500V. Considering our conductor as an External conductor, coated with a permanent polymer, from IPC2221A we derive the following calculations.

For 500 V the spacing between conductors needs to be 0.8mm, calculating for 750V we will need a spacing of 1.2575mm between the HV and HV Return & all other metal. The system will operate at 750V but tested for 1500V.

Resistance should be GΩ, or a current less than 1.5uA tested at 1500 V, for a dwell time of 30 seconds. The flex must be mounted on a metal vacuum jig, (isolated from its surroundings), held at HV to represent the sensor back plane of the final pixel module.

Electro-chemical migration according to IPC-TM-650 -2.6.14.1 needs to be measured and a safe value of resistance has to be derived for this measurement. This test is performed after HV test to confirm that HV testing has not degraded isolation characteristics.

* Over / under etch test: The traces on the PCB will be measured electrically or via optical inspection to confirm that they are neither over or under etched.

It could be difficult to measure the width of narrow lines accurately as it is not so clear under a microscope. In such cases precise resistance measurements for narrow and wide tracks can determine the effective width.

## Post Assembly

* In Circuit Test: Test performed after components are mounted on the pcb.
  + **Includes tests:** Open, Shorts above and measurement of component value used.
* High Voltage Test: This test will need to be performed again to avoid any issues due to solderability or contamination.
  + HV isolation of connector and HV filtering components are of particular interest.

# QA (Quality Assurance) in Industry

QA checks needs to be done on a Test token per batch in production.

## Impedance Control Test:

TDR (Time Domain Reflectometer) is used to check circuits to determine if the differential trace impedance is 100 Ω +/- 10Ω. Conductor length, spacing, width, height and separation affect the impedance. Polar Calculator is used in most cased to determine the above values.

In our design we will need to have controlled impedance for the high speed signal i.e. Data, Clk/Cmd.

This test is performed on test coupons (developed in industry for this purpose); these and reports will be provided by the manufacturer stating the impedance is achieved for the signals specified. This can be re-measured in the institute as described below.

## Cross-section of vias:

A cross-section of vias is made and the drill size and plating will be measured to ensure that it is within tolerances specified by the industry.

This test will be done on **Test Coupon-1**(design explained below).

# QC (Quality Check) at Institute

## Visual Inspection

* Check to ensure that the wire bond pads are clean and free from any deposit as this can affect the wire bonding process.
* Check for any shorts on the flex specially the connector on the bottom side of the flex.
* Check for Solder mask pealing or Cu etching if any.

## Metrology

Measure the size of the board, mounting hole positions to check that they meet the specifications. This will be measured in a non-contact coordinate measuring system, with a measuring accuracy of higher than 10um. Flatness will be measured on a non-contact coordinate measuring machine by measuring a defined number of points on the flex surface. The deviation of the surface must be below a given specification as required to allow the flex to be successfully glued to the pixel assembly. This value is still to be determined.

## Thermal cycling

The thermal cycling tests will be done on all flex circuits and on the test coupon mentioned below.

* Test coupon for thermal tests:

Test Coupon-1

This coupon with have multiple vias and long traces and will be built in the same panel as the flex. This coupon is designed to understand the effect of thermal cycling in via geometry, via to trace build quality including inter trace resistance.

Wire bond pads will be included to allow testing of the wire bond pull strength after rapid thermal cycles.

Layout for the test coupon is detailed in Appendix.

Procedure for thermal cycling is explained in IPC document -IPC-TM-650 -2.6.6

The test is conducted to determine the resistance of a printed circuit board to the shock of repeated exposure to extremes of high and low temperatures for a comparatively short period of time.

A chamber with automatic temperature cycling, compatible with the range of temperatures stated below need to be used for this test.

The specimen under test is cycled between temperatures as specified in table 1 for the said period of time for a total of 5 cycles continuously.

Once the PCB cools to room temperature, visual inspection and electrical testing is performed to see any obvious effects on the PCB due to thermal cycling including delamination of layers, cracked soldermask, inter trace isolation and trace resistance, wirebond pull strength, via electrical functionality.

The time to go from one temperature to the other, i.e. temperature ramp rate and the temperature range for operation has still to be defined for the flex under test. The test procedure does not specify the ramp rates and these have to be defined.

An example of thermal cycling temperature range as stated in the IPC document is defined in Table 1.

|  |  |  |
| --- | --- | --- |
| Step | Temperature(Deg C) | Time(Mins) |
| 1 | 125+3/-0 | 30 |
| 2 | 25+10/-5 | 10-15 |
| 3 | -65+0/-5 | 30 |
| 4 | 25+10/-5 | 10-15 |

Table

# QA (Quality Assurance) at Institute

## Signal Integrity

The impedance test coupon will be designed to be compatible with testing of the signal quality using the network analyzer.

Test Coupon-2

This coupon will be built in the same panel as the flex. The design will have an SMA connector that can connect to the network analyzer for measurements.

## Thermal Shocks and Continuity

Test Coupon -1 or a flex PCB or both are be used to do this test.

Procedure for thermal shocks is explained in IPC document -IPC-TM-650 -2.6.7.

The test is conducted to determine the physical endurance of printed circuit board to sudden exposure to extreme changes in temperature and the effect on the PCB due to the same. The exposure to these extreme temperatures is designed to cause physical damage, deterioration or significant change in resistance.

An automatic controlled dual temperature environmental test chamber or a similar dual chamber apparatus capable of maintaining temperature’s as specified in the IPC document stated above.

The specimen under test is cycled between temperatures as specified in Table 2 for the said period of time for a total of 100 cycles continuously.

|  |  |  |
| --- | --- | --- |
|  | Test condition D | |
| Step | Temperature(Deg C) | Dwell Time(Mins) |
| 1 | -55 +0/-5 | 15 |
| 2 | 25+10/-5 | 0 |
| 3 | 125+5/-0 | 15 |
| 4 | 25+10/-5 | 0 |

Table 2

The IPC document states “Transfer time between chambers shall be less than 2 minutes and the thermal capacity of the chamber shall be such that the ambient temperature shall reach the specified temperature within 2 minutes after the specimen has been placed in the chamber.”

The temperature range for operation and the number of cycles to run this test needs to be defined for the flex under test.

For the ATLAS ITK the expected rate of change of temperature is ≈1°C/s. Therefore a 10°C/s would give a reasonable temperature change rate.

Interconnect resistance measurement shall be taken before the test, during the first cycle at high temperature and during the last cycle at high temperature. Maximum change in resistance between the first and 100th cycle shall be evaluated.

## ENIG test

The **Test Coupon-1**or flex PCB can be used to perform this test. Bond pads are present on the flex PCB for this purpose. The coupon will be stressed to high current to check if gold migrates into copper depending on the nickel interface between two metals.

## Peal tests of the stack

Procedure for Peel strength of flexible printed wiring materials is explained in document IPC TM-650 2.4.9.D.

This test needs to be performed before and after thermal cycling and radiation testing. This will help in evaluating the base laminate material after the peel strength test is completed for degradation due to the thermal cycling and radiation exposure.

## Radiation tests

**Test Coupon-1**and**Test Coupon-2**can also be used for radiation testing. The connectors used on these coupons are screwed (not soldered) onto the PCB so can be removed during radiation tests.

This test needs to be done once on the build or if any material changes take place.

Radiation values are derived using the reference link below-

<https://twiki.cern.ch/twiki/bin/view/Atlas/RadiationBackgroundSimulationsExtendedAt4>

Total Ionising Dose (Gamma) of 3x 106 Gray, no safety factor is specified for the Endcap. Therefore irradiating to 6x106 Gray will includes a safety factor of 2.

For the inner region the specification states 107 with no safety factor.

The full range of thermal, mechanical and electrical tests will be performed after the radiation exposure during the design phase, first pre-production and if any material changes take place during production.

# Appendix

## Test Coupon Design

Both the test coupons described below will have the same build as that of the Pix Flex.

### Test Coupon-1

The coupon will have 150 vias (approximately 100 times the vias on the flex), double row of wirebond pads and traces.

The wire bond pads will be uniformly spaced to test bondability and pull strength over the area of the coupon.

It will have differential traces with 150um/150um trace width/trace spacing with serpentine routing.

A trace with 10 inches length with 18um Cu thickness and 150um trace width will measure a resistance of 1.6Ω.With a 1V supply a current of 625mA can measured using a Keithley 2410.

### Test Coupon-2

The test coupon will have two Samtec SMA (CCH-J-02) connectors which interface with the network analyzer. This connector is rated up to 20 GHz / 40 Gbps.

The SMA connector has a central signal pin with a ring of ground pins around it.

The connectors is screwed on the coupon for signal integrity testing and taken off for radiation testing. An optimal design is like the one shown below-



This test coupon will be 200mmX 30mm (approximately).This size is similar to the coupons built by industry for controlled impedance testing.