GU project status

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CEA-Leti-Minatec

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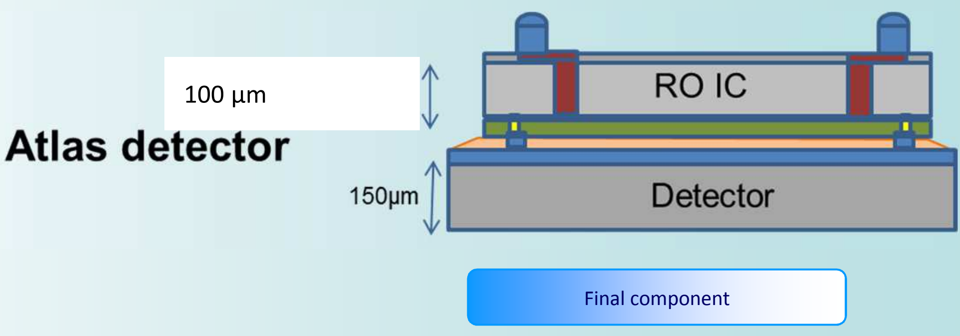
Customer initial requirements

- Objectives :
  - To supply thin wafers in order to test the dicing & the stacking of a detector on read out chip for ATLAS experiment
- Project requirements :
  - Process on FE I4 functional wafers / 200 mm
  - Need to have interconnects between ROIC and detector ➔ µbumps
  - Thin ROIC required ➔ 100 µm
  - Wafers debonding
  - Dicing & detector stacking will be done by Advacam (SME, spin-off of VTT)
  - Wafers bow measurements done by Scottish Microelectronic Center (SMC), GU leading
- Incoming wafers
  - Wafer diameter: 200mm
  - Wafer thickness: ~725um
  - IC Technology: 130 nm / IBM
  - Number of wafers provided: 10



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Process flow proposal – Runs 1 & 2

Incoming wafers

Front side µbumps

RUN 1 : delivering of two wafers to Advacam

Temporary bonding

Thinning to 100 µm

Debonding

Taping & delivering to SMC for bow measurements

RUN 2 : delivering of two debonded thin wafers to SMC

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Process flow proposal – Run 3: R&D

Incoming wafers

Front side µbumps

Temporary bonding

Thinning to 100µm or more if needed

Stress compensation layer

Debonding

Taping & delivering to SMC

RUN 3 : delivering of two debonded thin wafers + stress compensation layer to SMC

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Process flow proposal – Runs 4 & 5 : R&D

Thinning to 100µm or more if needed

Optimized Stress compensation layer

Debonding

Taping & delivering to SMC

RUN 4 : delivering of two debonded thin wafers + stress compensation optimized layer to SMC

RUN 5 : delivering of two debonded thin wafers + stress compensation optimized layer to Advacam

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LETI proposal

- **Technical proposal**
  - Layout of Micro-bumps level
  - **RUN 1** : Delivery to Advacam of two FE I4 wafers with µbumps on front side / without thinning (725 µm) ➔ **D1**
  - **RUN 2 :** Delivery to SMC of two FE I4 thinned wafers (100 µm) + µbumps on front side **– D2**
  - **RUN 3 :** Delivery to SMC of two FE I4 thinned wafers + backside stress compensation + µbumps on front side ➔ **D3**
  - **RUN 4 :** Delivery to SMC of two FE I4 thinned wafers + Optimized backside stress compensation + µbumps on front side ➔ **D4**
  - **RUN 5 :** Delivery to Advacam of two FE I4 thinned wafers + Optimized backside stress compensation + µbumps on front side ➔ **D5**
  - Optimized thickness of Si will be adapted after run2 if needed (150µm possible).
  - Stress compensation layer will be chosen in the LETI materials according to SMC wafer bow/warpage measurements / One single trial, no specific stress study.
  - Every functional wafers will be chipped with dummies wafers.

- **LETI needs :**
  - GDS files of FE I4 chips : top metal & passivation
  - FE i4 Wafer mapping / wafer step plan
  - Layer table
  - Ten FE I4 wafers (10)

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Planning & deliverables proposal

- Proposed planning / 8 months duration

	Task	Owner	Month 1	Month 2	Month 3	Month 4	Month 5	Month 6	Month 7	Month 8
FE I4 wafers	µbumps Layout & masks	Open 3D								
	3D Technology run 1	Open 3D								
	3D Technology run 2	Open 3D								
	3D Technology run 3	Open 3D								
	3D Technology run 4	Open 3D								
	3D Technology run 5	Open 3D								
	Bow measurement	SMC								
	Dicing - Stacking	Advacam								
	Deliverables	LETI - Open 3D				D1	D2	D3	D4	D5

- Deliverables :
  - D1 : µbumps GDS files + 2 FEI4 wafers (725µm) with µbumps on front side
  - D2 : 2 thinned FEI4 wafers to 100 µm with µbumps on front side / debonded on tape
  - D3 : 2 thinned FEI4 wafers to 100 µm with µbumps on front side + stress compensation layer / debonded on tape
  - D4 : 2 thinned FEI4 wafers to 100 µm with µbumps on front side + optimized stress compensation layer / debonded on tape
  - D5 : 2 thinned FEI4 wafers to 100 µm with µbumps on front side + stress compensation layer / debonded on tape / Advacam

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Financial proposal

- Financial proposal :
  - µbumps design, layout & mask
  - 3D technology on ten FEI4 wafers provided by Glasgow University including :
    - µbumps on front side
    - Temporary bonding
    - Si thinning
    - Stress compensation layer implementation
    - Debonding & taping
    - Shipping to SMC and Advacam
  - Five different runs

- Total price : **97 000 €**
- Payment conditions :
  - 36 000 € @ 31/03/2013
  - 61 000 € @ the end of the project

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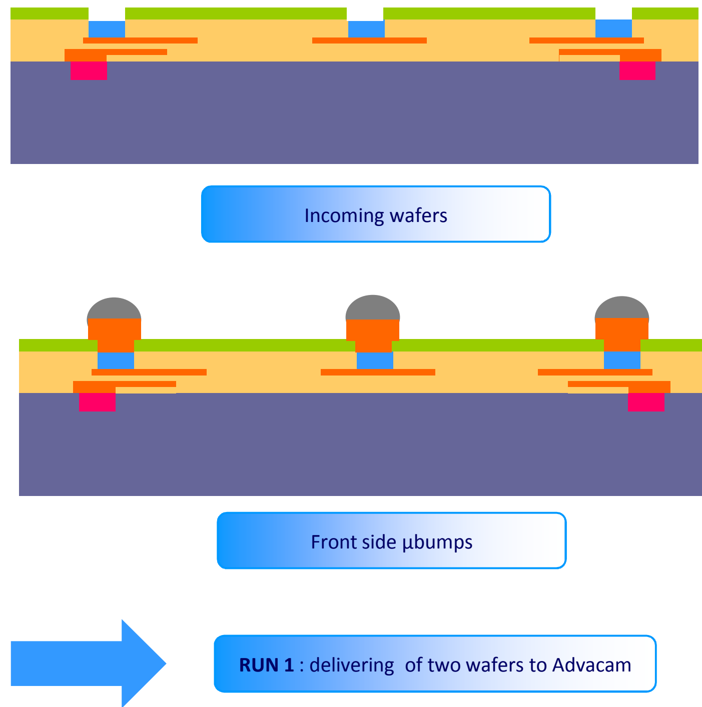
RUN1 results



- 2 wafers with copper µbumps
  - Start date = 8/03/13
  - Shipping date to advacam = 23/04/13

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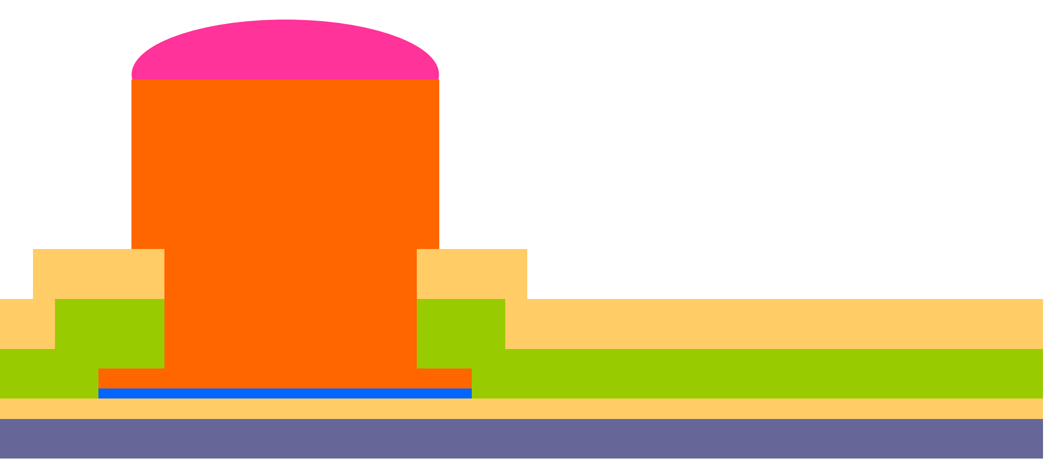
Process Flow



- -Control
- -Back side and front side cleaning
- -Preclean + seed layer deposition Ti 100nm + Cu 400nm
- -Photolithography « µBump », negative photoresist
- -Flash O2
- -ECD Cu 10µm + SAC 8µm
- -Stripping
- -Cu 400nm + Ti 100nm wet etch
- -SAC reflow

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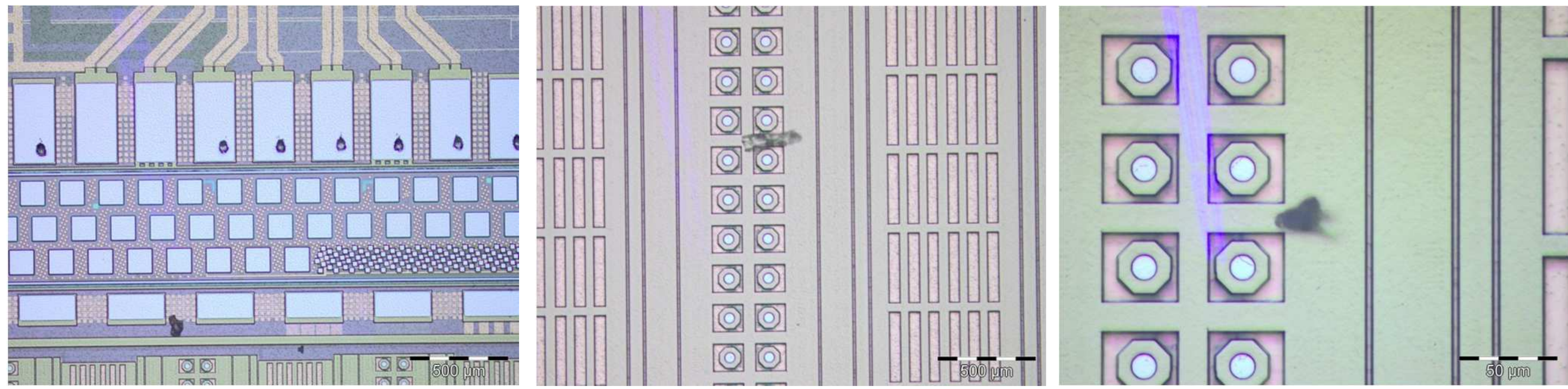
Control before process



Observations before process

- 2 wafers provided by Glasgow university
- Control before process: some particles have been observed
- A front side specific cleaning has been performed ➔ number of particles decreased

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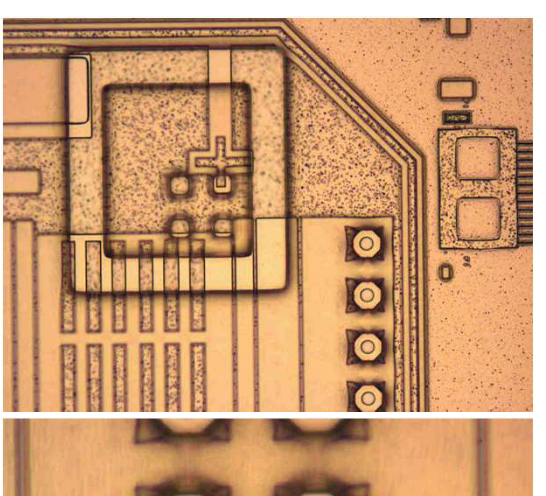
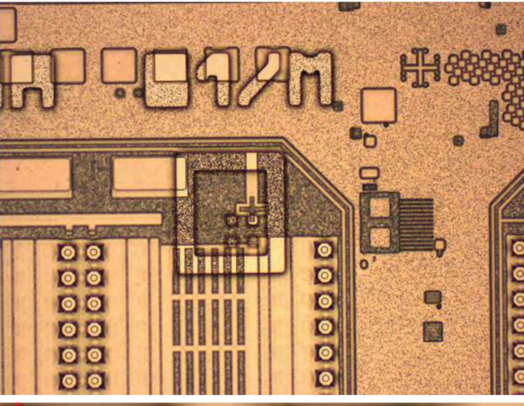
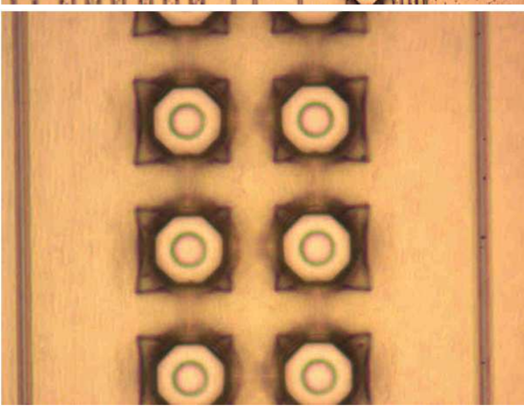
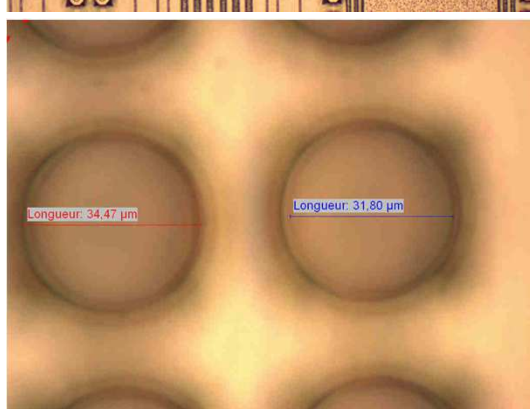
µBump litho





Observations after the photolithography step





- The position of alignment marks designed by LETI is not correct
- Alignment of µbump level has been performed on the metal pads directly
  ➔ OK
- µbump diameter=30µm

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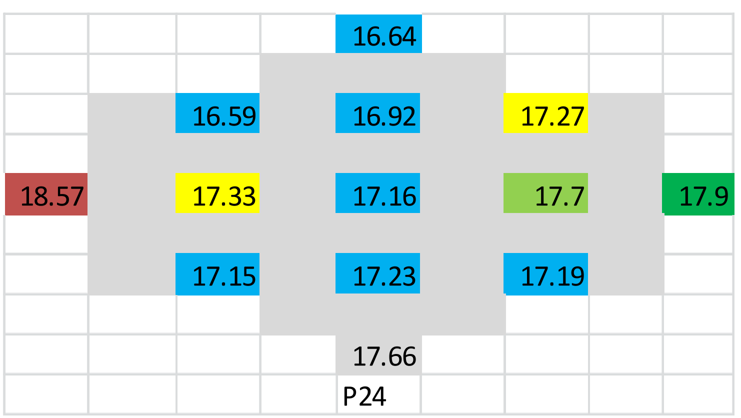
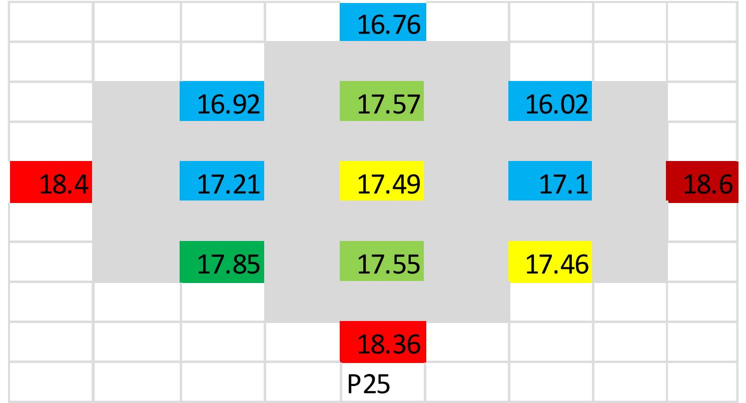
µBump ECD Cu-SAC





µbumps height measurements after ECD step (wafer map on the 2 wafers)

- ECD Cu 10µm + SAC 8µm
- Strip + µbump height measurements:
  - P24: mean=17.33µm – unif = 3.18%
  - P25: mean=17.48 – unif=4.08%

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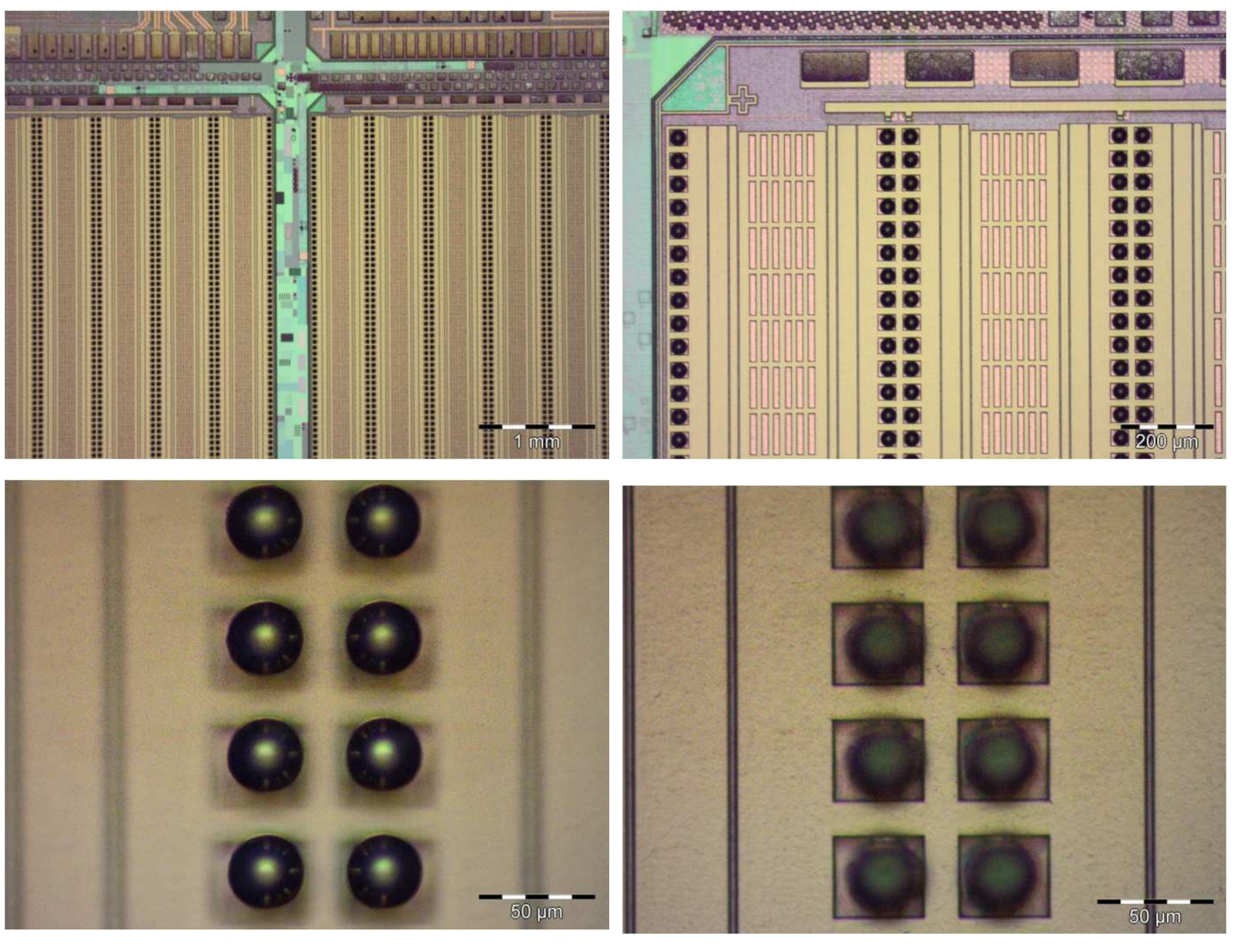
µBump after SAC reflow



Observations after SAC reflow

- Seed layer etch + SAC reflow
- 2 probes resistance measurement =~2.5 Ohm on 2 µbump chain on top metal

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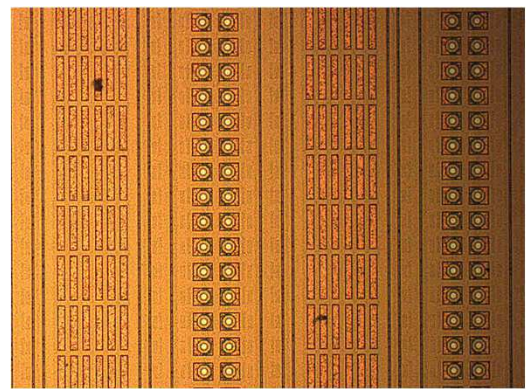
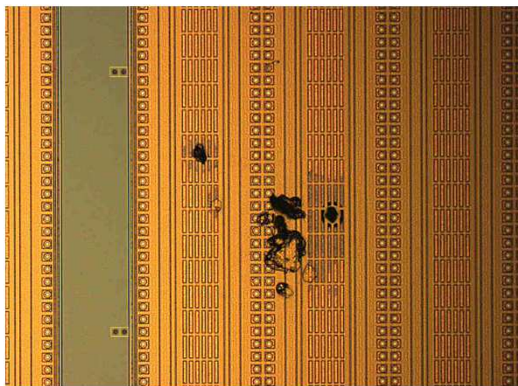
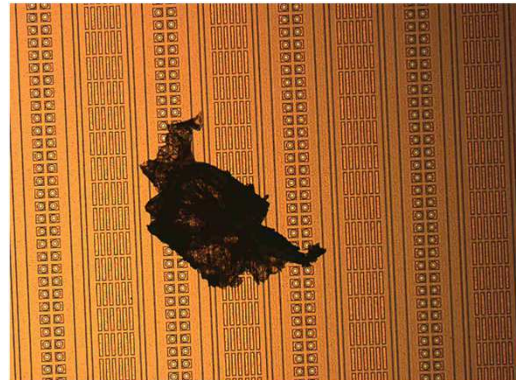
RUN2/3 status

- 4 wafers with copper µbumps + temporary bonding + thinning 100 µm + stress compensation (run 3)
  - Start date = 12/04/13 (1 month delay vs RUN1)
  - Incoming inspection = some big particules







  - Current status = @ seed removal after µbump Cu/SAC ECD
- Short loop with µbumps/Si monitors for temporary bonding and thinning setup in progress

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RUN4&5

- Waiting 4 remaining wafers from GU → planning will be shifted accordingly

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Temporary bonding solutions

- Move from Brewer HT10.10 Science slideoff to BSI ZoneBond technology

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Wafer bonding in LETI

- Permanent Bonding (with or without alignement)
  - Direct bonding (Oxyde, Metallic)
  - Anodic Bonding
  - Metallique Thermocompression
  - Eutectique Bonding
  - Polymer Bonding

- Temporary Bonding (without alignement)
  - Zone Bond Process
  - 3M WSS Process

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Temporary Bonding

- Requirement
  - Bonding with important topology
    - 10-60µm of electrical bumps
  - Thinning down to 50-100µm
  - Backside processing @200°C
  - Cold debonding
  - Good throughput
  - “Universal”

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Temporary Bonding

- Zone Bond Process

Device

Gluing

Bonding

Thinning and back processing

ZoneBOND Carrier

Carrier Recyclage

Edge wet chemical etching.

Debonding

Taping

Dicing and Pick and place

Cleaning

- Before debonding -

Frame

Device

Glue

Carrier

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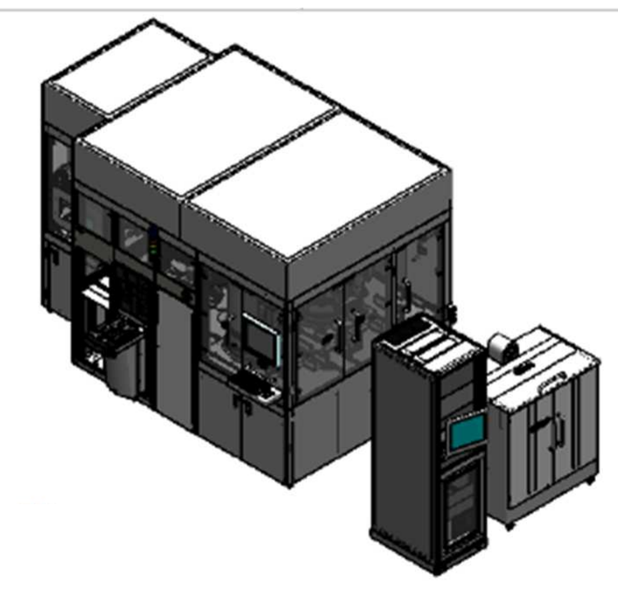
Temporary Bonding

- Zone Bond Tool

Bonder



Debonder

CONFIDENTIAL

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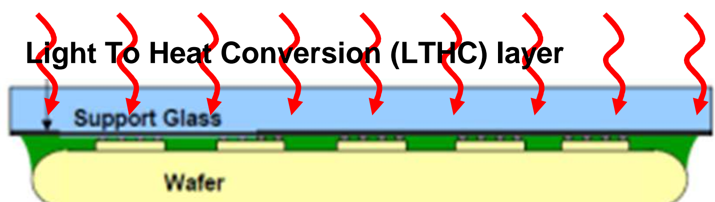
Temporary Bonding

- WSS 3M Process

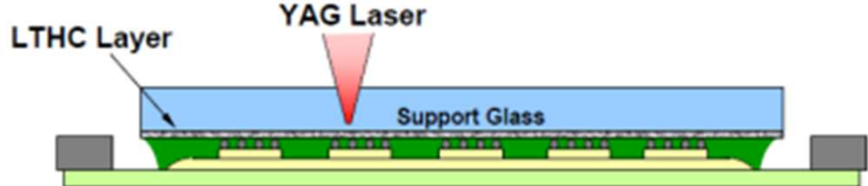
Device Gluing

LTHC carrier bonding and UV curring

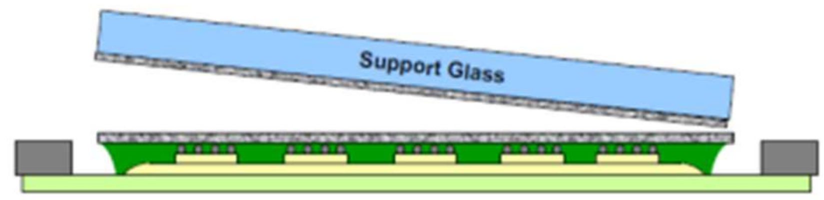


Back thinning, processing and taping

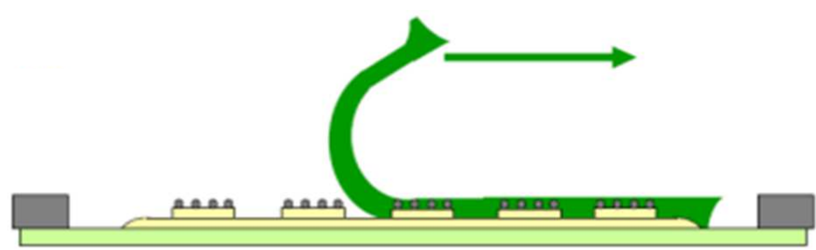
Laser lift-offf



Mechanical carrier debonding



Glue peel off using speifique tape



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Temporary Bonding

- Yushin Tool

Bonder

Debonder

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Temporary Bonding

- Advantages and challenges
- ZoneBOND:
  - Glue choice
  - **Silicon carrier or transparent carrier**
  - **Chemical polymer cleaning after debonding**
  - Chemical resistance of the tape
  - Low bonding energy
  - Specific carrier (availability, cost)
  - **New debonding tool**

- WSS 3M
  - **Cured polymer**
  - Important bonding energy
  - Tool maturity
  - Specific polymer
  - Polymer residues after debonding
  - Specific LTHC treatment (availability, cost…)
  - None transparent glass wafer

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Pick& place at LETI

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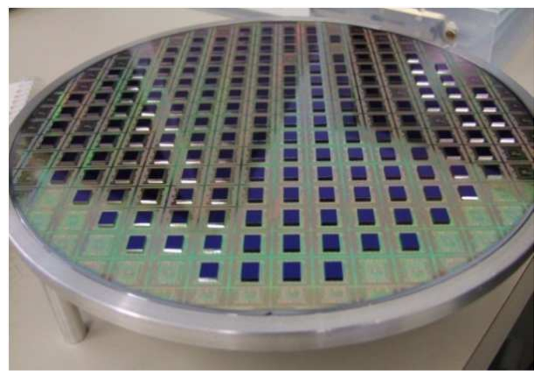
Pick & Place tools at LETI

Datacon 2200 apm+

Panasonic FCB3



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Tool specifications

	Datacon 2200 apm+	Panasonic FCB3
Alignement accuracy (3σ)	±7µm	±3µm
Bonding speed (units/h)	2000 @ ±7µm 3000 @ ±25µm 1000 @ ±7µm with dispensing or dipping	2000 @ ±3µm
Bonding force	1-50N	5-490N
Chuck temperature (substrate)	Up to 250°C	Up to 150°C
Bond head temperature (chip)	Up to 350°C	Up to 500°C
Bonding cycle complexity (time, temperature, force)	Single step available (only one set of parameters during the cycle)	Multiple steps available
Substrate size	Up to 200mm diameter <3mm thickness	Up to 300mm diameter <3mm thickness
Chip size	0.8x0.8 up to 25x25mm²	1x1 up to 20x20mm²
Flip chip unit	Available	Available
Chip packing for pick-up	Wafer/tape Waffle pack Gel-pak®	Wafer/tape Waffle pack (flip mandatory) Gel-pak® (no flip available)
Dispensing unit	Available	Available
Dipping unit	30 and 50µm depth	20µm depth

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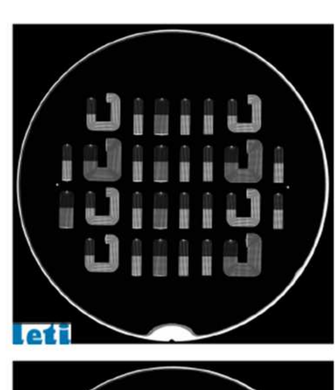
Micro fluidic passive interposer (project with CERN)

- Direct bonding with main steps:
  - Surface preparation (critical): Hydrofilic or hydrophobic
  - Bonding under vaccum
  - Baking at high temperature
  - SAM control
  - Test under high pressure > 100 bar

P05



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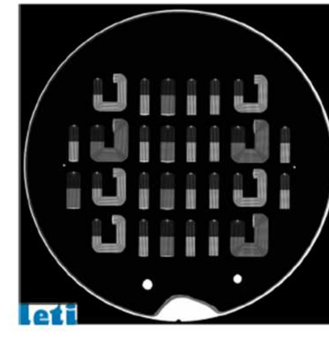

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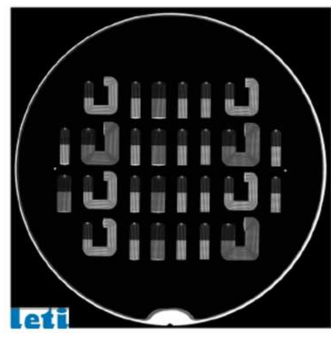

P08

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Open 3D™ technological offer

- **Technological modules définitions :**
  - TSV
  - RDL
  - Interconnections
  - Stacking
  - Packaging with partner collaboration

Top die

Front side UBM

Bottom die or interposer

RDL

Back side UBM

Micro-bumps

Landing micro-bumps

TSV

Passivation

Pillars

Landing pillars

Substrate or BGA or package

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Open 3D™ technological offer

Technological modules

TSV Last

AR 1:1	AR 2:1	AR 3:1

Interconnections

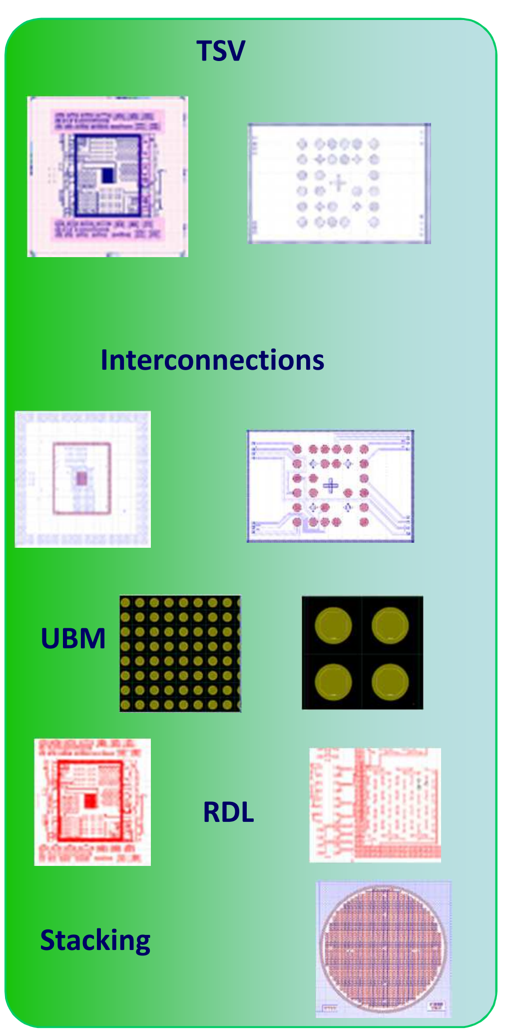
Micro-bumps	Landing micro-bumps	Pillars

Under Bump Metallurgy (UBM)

Redistribution layer (RDL)

Stacking : D2W

DRM / DK / layout / masks



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Open 3D™ technological offer / TSV

TSV Gallery

TSV diameter	30 µm	40 µm	50 µm	60 µm
AR 1:1 & 1.5:1				
AR 2:1	Not yet demonstrated		Available Not yet required	
AR 3:1	Not yet demonstrated		Available Not yet required	Not yet demonstrated

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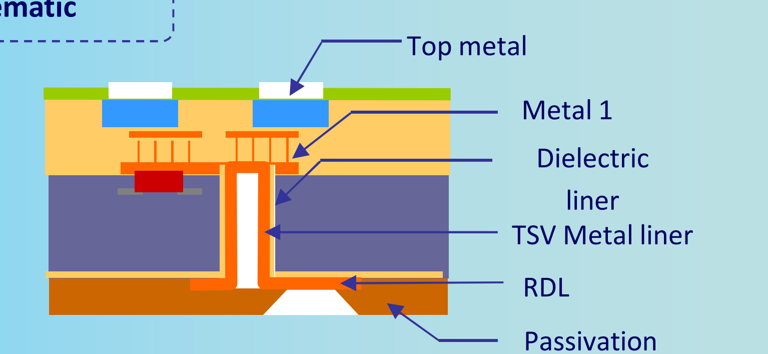
Open 3D™ technological offer / TSV

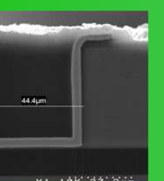
TSV DRM & schematic

- Wafer size : **200 & 300 mm**
- TSV type : **via last / Cu liner**
- Minimum pitch : **80 µm (for 40µm TSV)**
- TSV diameter : **40 to 100 µm**
- Aspect Ratio (AR) : **from 1:1 to 3:1**

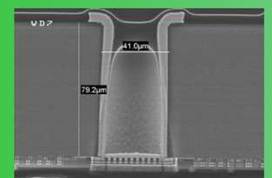


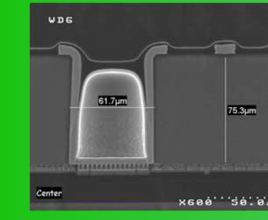
TSV morphological & electrical results

AR 1:1

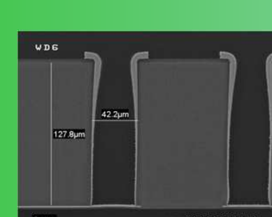


AR 2:1



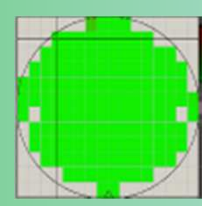


AR 3:1

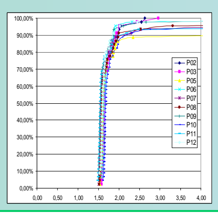


TSV characteristics

TSV geometry	R (mΩ)	C (pF)	Elec. Yield	Insul. (MΩ)	I_{leak} (A)
$TSV_{60/80}$	15.1	0.57	100 %	> 100	-
$TSV_{60/120}$	19.1	0.82	100 %	> 100	$1.3\ 10^{-9}$ **@ 10V** $3.1\ 10^{-9}$ **@ 50V**
$TSV_{40/80}$	20.1	0.46	> 99%	> 100	-
$TSV_{40/120}$	30.4	0.63	> 99%	> 100	$7.4\ 10^{-9}$



Electrical tests results



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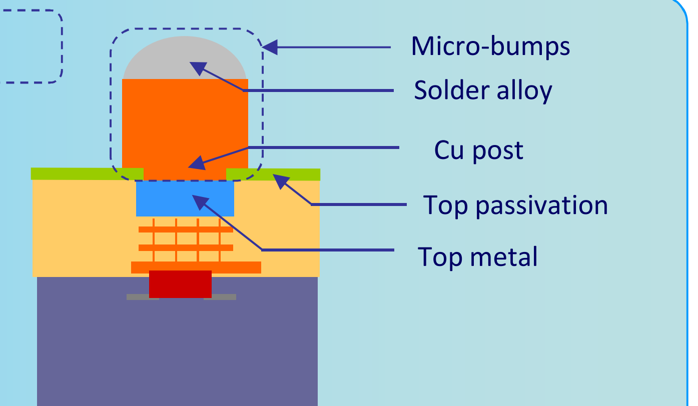
Open 3D™ technological offer / Micro-bumps

Micro-bumps DRM & schematic

- Wafer size : **200 & 300 mm**
- Micro-bumps material : **Cu post / SnAg solder**
- Minimum pitch : **50 µm**
- Micro-bumps diameter : **25 µm**
- Micro-bumps thickness : **Cu 17µm / SnAg 10µm**



Micro-bumps Morphological & electrical results

Micro-bumps before reflow

Micro-bumps after reflow

Micro-bumps characterization

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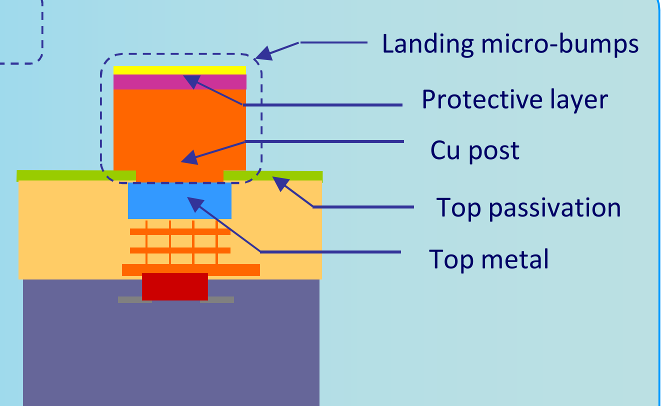
Open 3D™ technological offer / Landing micro-bumps

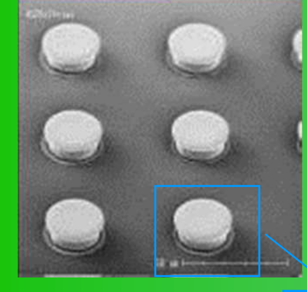
Landing micro-bumps DRM & schematic

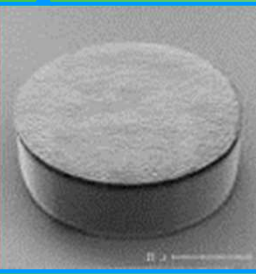
- Wafer size : **200 & 300 mm**
- Landing micro-bumps material : **Cu post / NiAu protection possible**
- Minimum pitch : **50 µm**
- Landing micro-bumps diameter : **25 µm**
- Landing micro-bumps thickness : **Cu 10µm / NiAu 1.2µm**



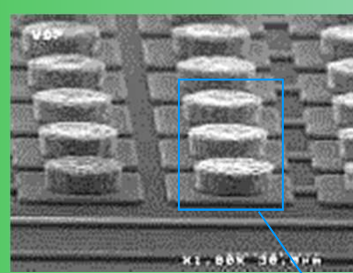
Landing micro-bumps Morphological & electrical results

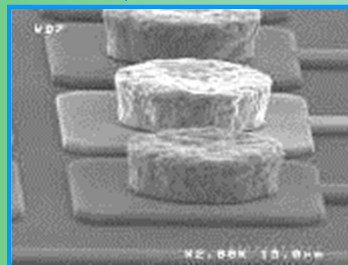
Landing micro-bumps with protective layer



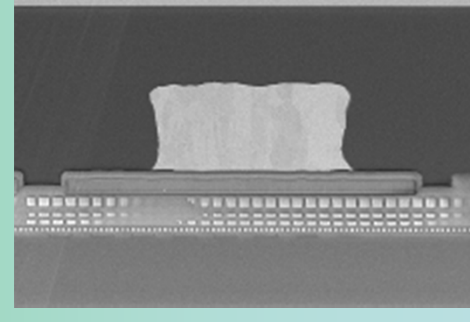


Landing micro-bumps w/o protective layer





Landing micro-bumps on top metal



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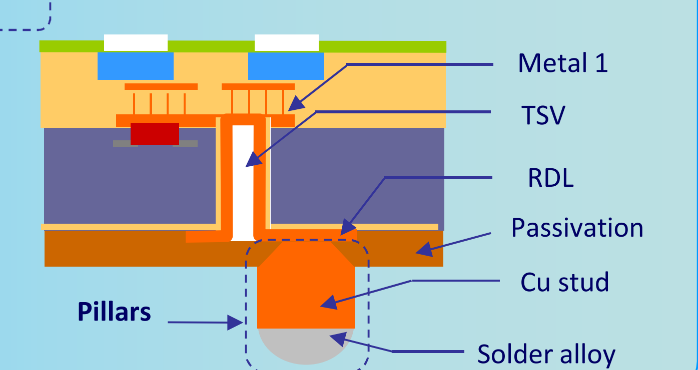
Open 3D™ technological offer / Pillars

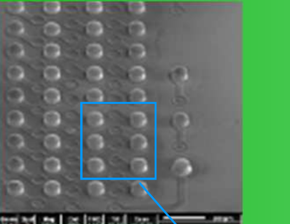
Pillars DRM & schematic

- Wafer size : **200 & 300 mm**
- Pillars material : **Cu stud / SnAg solder**
- Minimum pitch : **120 µm**
- Pillars diameter : **60-80 µm**
- Pillars thickness : **Cu 35-40 µm / SnAg 25-30 µm**

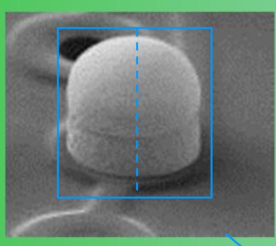


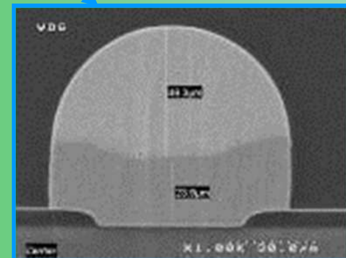
Pillars Morphological & electrical results

Pillars



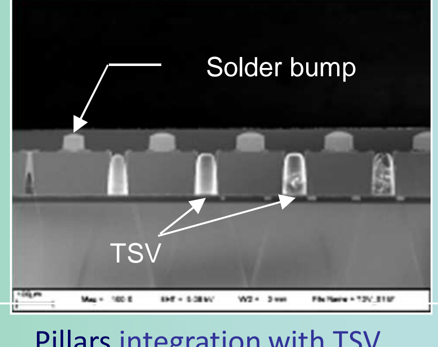
Pillars cross section





Pillars characteristics

	R (mΩ)	Elec. Yield
Pillars	50	100 %



Pillars integration with TSV

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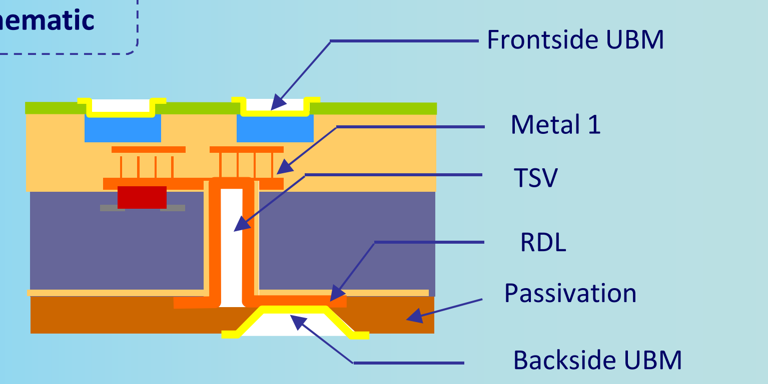
Open 3D™ technological offer / UBM

UBM DRM & schematic

- Wafer size : **200 & 300 mm**
- UBM material : **TiNiAu**
- UBM thickness : **0.5 – 10 µm**
- UBM minimun width : **30 µm**
- UBM minimun pitch : **60 µm**



UBM Morphological & electrical results

Backside and frontside UBM possible

Different shape possible :

- Square
- Polygons
- Circle

Two possible technologies :

- Metal sputtering / thickness range : 0.5 – 1 µm
- ECD / thickness range : 1 – 10 µm

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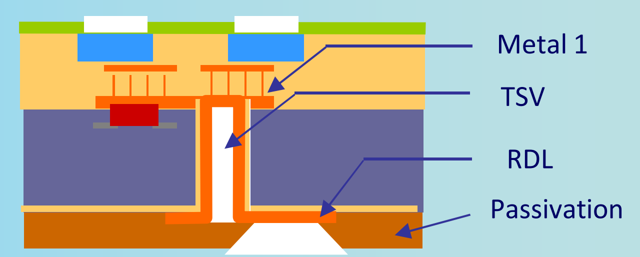
Open 3D™ technological offer / RDL

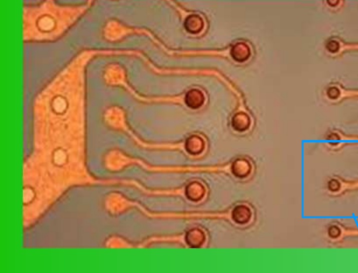
RDL DRM & schematic

- Wafer size : **200 & 300 mm**
- RDL material : **Cu / protective layer possible**
- RDL thickness : **1-10 µm**
- RDL minimun width : **20 µm**
- RDL minimun space : **20 µm**



RDL Morphological & electrical results

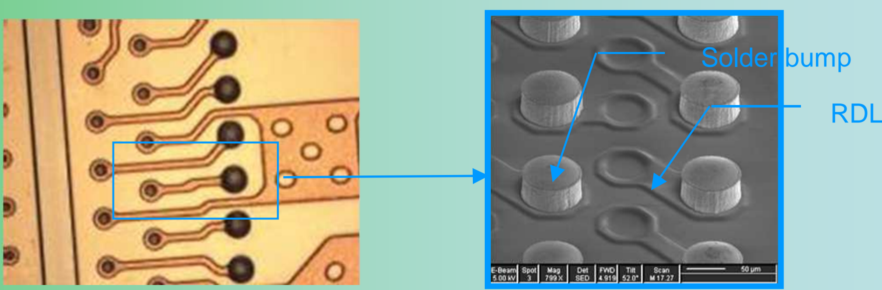
Backside Cu RDL



RDL characteristics

	Insolation between lines	I_{leak} @ 10V (A)	Elec. Yield
RDL	> 6.0 GΩ	1.6 10^{-9}	100 %

Cu RDL integration : Solder bumps on RDL + passivation



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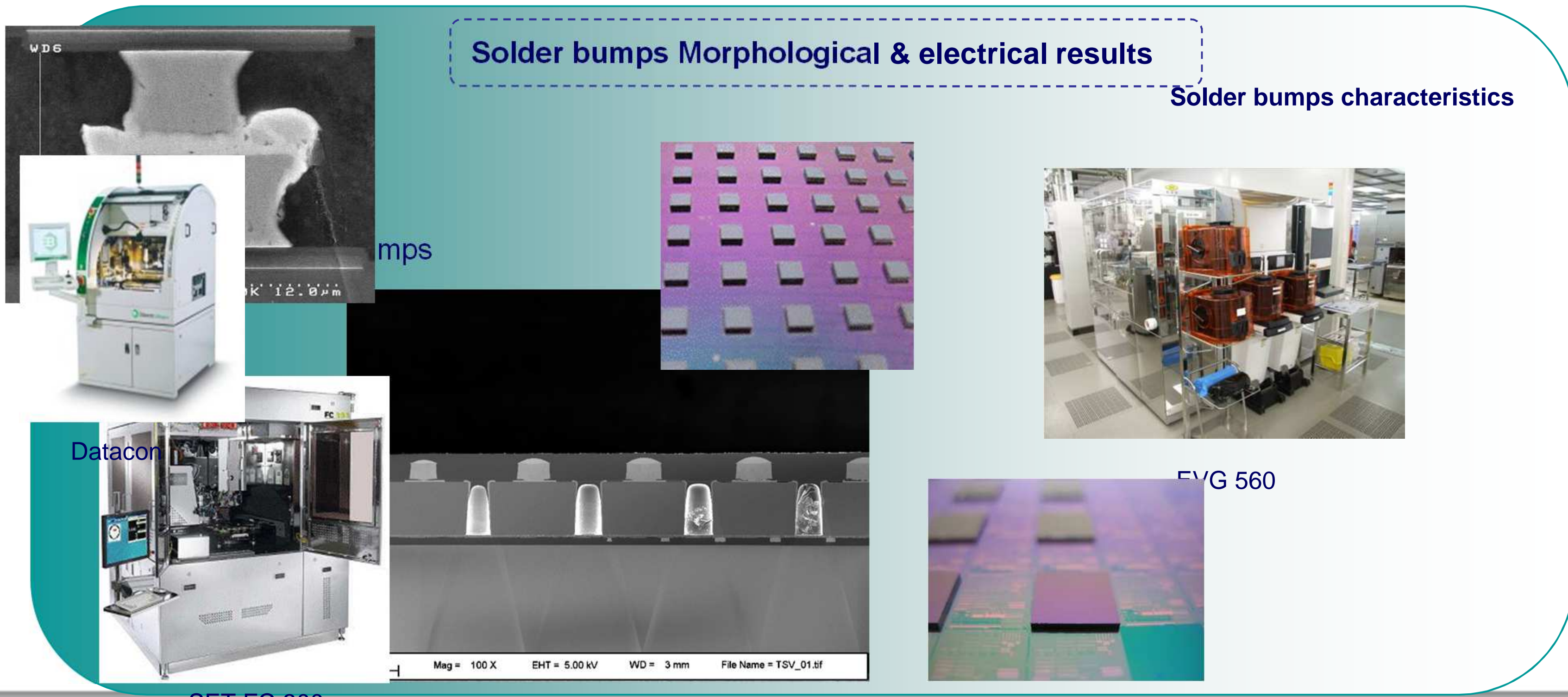
Open 3D™ technological offer / Stacking

Solder bumps DRM & schematic

- Wafer size : **200 & 300 mm**
- Solder bumps material : **Cu stud / SnAg solder**
- Minimum pitch : **120 µm**
- Solder pillar diameter : **60-80 µm**
- Solder pillar thickness : **Cu 35-40 µm / SnAg 25-30 µm**

Solder bumps Morphological & electrical results



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Cost estimation for full interposer

process steps
Seed deposition Ti/Cu
Photo µbumps FS
ECD Cu/SAC
Stripping
Seed Cu/Ti etch
Reflow
Glue spin coating
BONDING
GRINDING (4 steps)
CMP
LTO Déposition
VIAS Photo
VIAS HM etch
VIAS Si etch
VIAS PMD etch
PASSIVATION Deposition
PASSIVATION Gravure
VIAS Stripping
CONTACTS Photo
CONTACTS etch
CONTACTS Stripping
Seed deposition Ti/Cu
RDL Photo
RDL Cu ECD
RDL Stripping
RDL anneal
SEED LAYER etch
ELECTRICAL TESTS
PASSIVATION Photo
ELECTRICAL TESTS
UBM deposition
Photo UBM
UBM etch (4 steps)
Stripping
Debonding
Cleannig glue
Dicing tape mounting
Dicing chips
Tape UV release
Chips pick out
handling and box packaging

- 66 main steps
- Estimate cost (not contractual) for 10 wafers = 150 kEuros
- for 1000 wafers need more feasibility study for cost evaluation and processing capability

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Thank you for your attention