Design specification – Atlas MCMD strip hybrid

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Version 0.5 (Draft – not for implementation!)

Abstract:

This document is a design specification of a front-end hybrid circuit for the Atlas strip tracker upgrade, implemented in MCMD technology. The design is based on the existing kapton hybrid; in particular the external interface and dimensions are kept identical. The details of the current kapton hybrid are given in the appendixes and this document should provide sufficient background and details to fully define the design of the MCMD hybrid.

Table of Contents

List of Figures

List of Tables

1. Introduction

The fist step in our evaluation of MCMD technology for silicon strip sensors had the purpose of studying the influence of MCMD post-processing on the sensor wafers. This was done by depositing one dielectric and one metal layer on sensor wafers of electrical and mechanical grade. The electrical wafers contained fully functional silicon strip sensors. This step was successful and the measured change in characteristics was small, only non-negligible effect was an increase in total capacitance of the sensing strips. This was expected from the presence of an additional ground plane close to the strips.

The next step in the evaluation of this technology is to build a fully working front-end circuit, which acts as the interface between the sensor, front-end ASICs and passive components and provides the connectivity to the external world. This type of circuit is normally referred to as a 'multi-chip module' in the electronics industry and is known as a 'hybrid' in the particle physics community. The baseline design of this circuit is implemented on a flexible kapton circuit with four metal layers plus one metal screen layer. It is glued on to the silicon sensor and could potentially be replaced by a MCMD based circuit.

The first prototype of the MCMD hybrid will be implemented on blank 6-inch silicon wafers. The wafers should be 300 μm thick and be provided by Acreo. The cost for the blank wafers should be included in the quote. The connections to the silicon strips will be omitted from this first design. The electrical functionality and layout of the MCMD hybrid should be as close as possible to the ones of kapton hybrid. In particular, the physical format, ASIC positions and electrical interface should be kept identical. The schematics, the layout files in Gerber and DXF format and a specification of the front-end ASIC are supplied as appendixes to this document for reference.

2. Quote specification

This document is a design specification for layout and processing at Acreo. The requested quote should include:

- Eight blank silicon wafers of thickness 300 μm.
- Layout of the circuits as specified in this document
- Eleven masks plates needed for processing
- Two iterations of the processing as specified in this document, with four wafers in each batch.
- Review of processing after the first iteration, with the possibility to drop the shield layer and one BCB layer in the second iteration.

3. Wafer level design

3.1. Layout overview

The silicon micro-strip sensors are 97.6 x 97.6 mm^2, processed on 6-inch wafers as indicated by the dotted rectangle in Figure 1. The sensors have four rows of 1280 strip implants, with a pitch of 75 μm and length of 2.5 cm. Each row is read-out by 10 front-end ASICs with 128 channels each. They are arranged on two identical circuits, each one with two rows of ASICs. The locations of the circuits are shown in Figure 1, labelled 'Hybrid 1' and 'Hybrid 3'. Each hybrid circuit is 24 x 107.6 mm^2 and the clearance to the edge of a 6-inch wafer is 9.3 mm.

The external connections to the circuits are done via arrays of bond pads at the two ends of the circuits.

Since the first prototype run is done on blank wafers, no strip connections are needed. Hence the area between the two hybrids is empty and can be used for an additional, identical hybrid circuit labelled 'Hybrid 2' in Figure 1. This circuit is added to increase the number of available circuits after processing and wafer dicing.

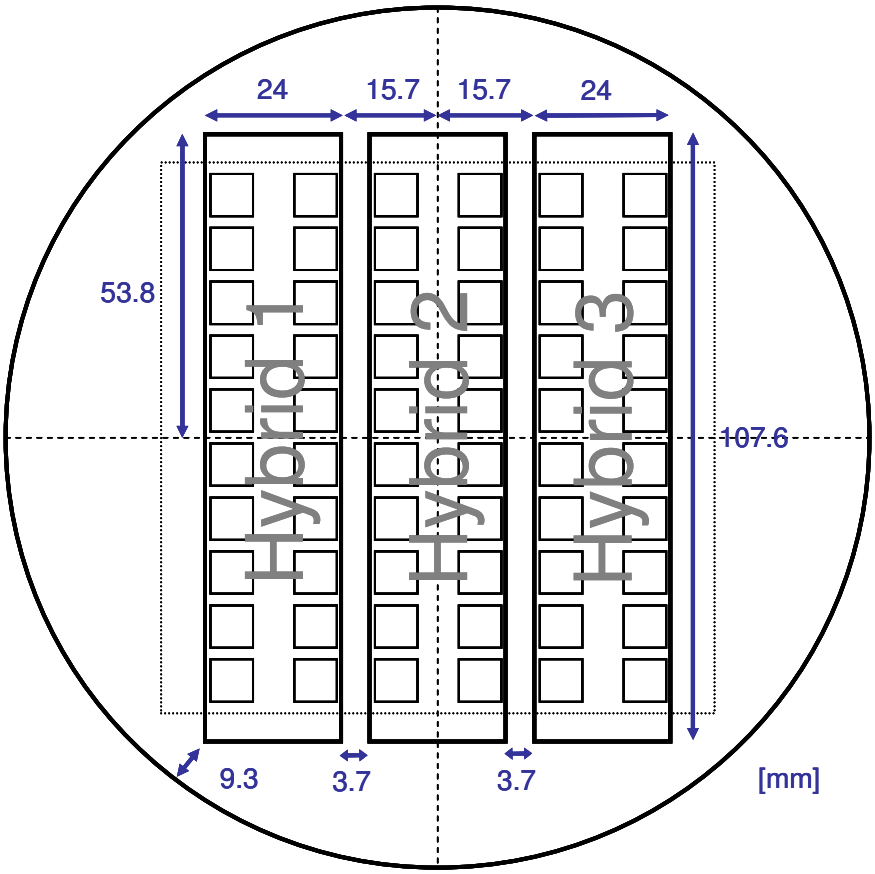

Figure 1: The figure shows an overview of the wafer, with the three identical hybrids positioned as shown. The dashed lines indicate the two symmetry lines of the wafer and the dotted rectangle indicate the active sensor area on electrical wafers.

3.2. Layer stack-up

The layer stack-up of the MCMD hybrid is similar to the kapton hybrid, but with a significant difference in layer thicknesses. The layers should be as follows

1. 12 μm BCB. Dielectric insulation between sensor and first metal layer. No patterns apart from the saw streets in the first prototype run.
2. 1 μm Cu/Ti. Screen to shield the sensor from noise induced by the fast signals on the hybrid. Meshed plane with 50% area coverage and 30x30 μm^2 openings. The screen should have the same size and shape as the ground and supply planes.
3. 2-3 μm BCB. Dielectric insulation, exact thickness chosen to maximise process success probability.
4. 2 μm Cu/Ti. Solid ground plane for power distribution to the ASICs, with small openings to allow the layers below to breath. Openings should be less than 10% of the surface area and have shapes to maximise conductance in the length direction of the hybrid.

5. 2-3 μm BCB. Dielectric insulation, exact thickness chosen to maximise process success probability
6. 2 μm Cu/Ti. Solid supply voltage plane for power distribution to the ASICS, with small openings to allow the layers below to breath. Openings should be less than 10% of the surface area and have shapes to maximise conductance in the length direction of the hybrid.
7. 3-10 μm BCB. Dielectric insulation. Thickness tuned to achieve the correct differential line impedance.
8. 1 μm Cu/Ti. Signal layer for trace routing
9. 2-3 μm BCB. Dielectric insulation, exact thickness chosen to maximise process success probability.
10. 1 μm Cu/Ti. Signal layer for trace routing and components
11. 2-3 μm BCB. Passivation layer, exact thickness chosen to maximise process success probability.
12. 3 μm Ni plus flash Au layer. For ultrasonic bonding with Aluminium wire and for soldering of passive components.

Layers 1 and 2 could be omitted the in the second processing iteration if the first fails. Exact alternations will be defined by a review in case of a failure of the first batch.

3.3. Saw streets

Saw streets are required in the BCB and metal layers for dicing the wafers to avoid cracking of the BCB by the cutting process. The required width is 400 μm at the bottom of the saw street and then widened slightly for each layer, according to Acreo's standard layout rules. The wafer will either be cut up as three separate hybrids or along the envelope of the silicon sensor and hybrid assembly. The locations of the saw streets are indicated in Figure 2.

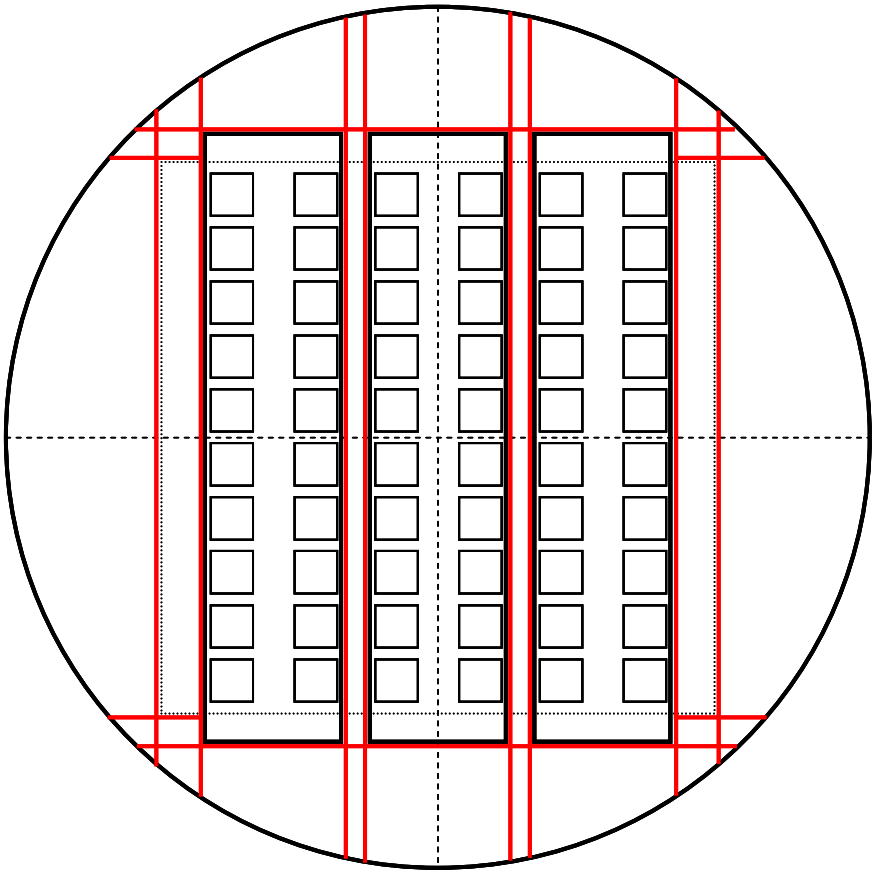

Figure 2: The figure shows the location of the saw streets, indicated by the red lines. They should be implemented outside the envelope of the hybrid and sensor outlines.

3.4. Alignment marks

Acreo should implement their standard alignment marks on each layer of the build, as needed by the processing.

3.5. Test structures

The areas outside the envelope of the electrical sensors can be used for test structures to monitor the quality and performance of the processing. Acreo is encouraged to use this are for their standard test structures to monitor the process.

4. Hybrid design

4.1. ASIC positions and footprint

The hybrid should be 24 x 107.6 mm², with its outline indicated by the red brackets in Figure 3. The figure shows the top two layers in green and blue with the foot prints of the ASICs in two rows, traces for signal routing and pads for surface mount components and wire bonding. The distance from the hybrid edge to the centre of the first ASIC is 4.35 mm in the narrow direction and 10.6 mm in the long direction. The distance centre-to centre between the ASICS is 9.6 mm. Further dimensions can be extracted from the supplied Gerber and DXF files.

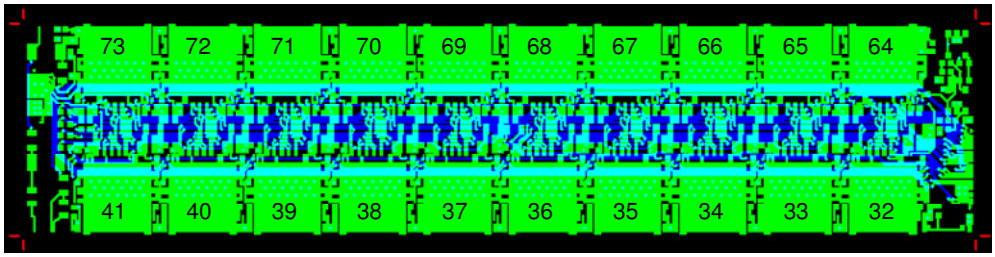

Figure 3: The Gerber screen shot shows the layout of the two signal layers of the current kapton hybrid. Numbers indicate chip addresses and are referred to in the text describing signal routing. The control end is to the right and the power end is to the left in the picture.

Figure 4 shows the foot-print of the front-end ASIC on the current kapton hybrid. The ASIC is mounted on a solid ground pad, surrounded by bond pads for the ASIC connectivity described in Section 5. There are two alignment marks used for mounting the ASICS, seen in Figure 4 with the shapes of an 'F' and a '+'. The exact footprint can be extracted from the supplied Gerber and DXF files.

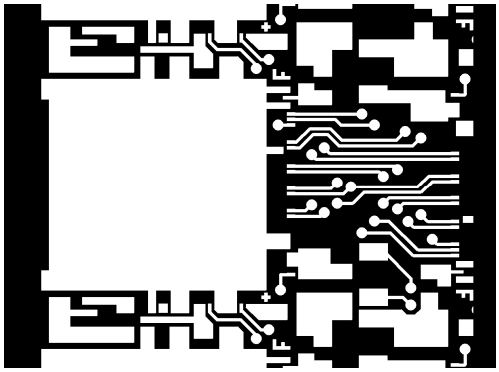

Figure 4: The Gerber screen shot shows the foot print of the ASIC in layout of the current kapton hybrid.

4.2. Low voltage supply

The power and high voltage connections to the hybrid are located at one end and are made via wire bonds to an interface board. Figure 5 shows the top layer of this part of the current kapton hybrid. The external interface should be kept identical in the MCMD hybrid and the required functionality should be implemented in this area.

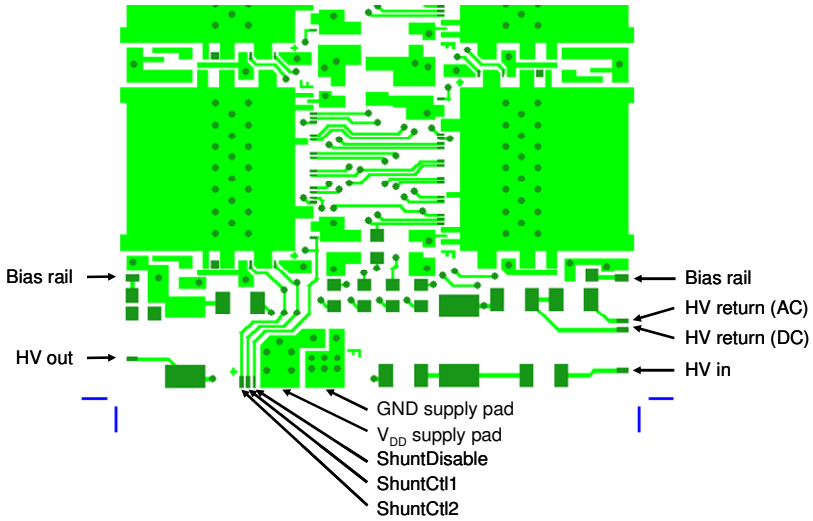

Figure 5: The figure shows the implementation of the supply connections and the high voltage filter. It also shows the location of the bond pads for sensor bias and the connection between ground and shield planes.

The low voltage is supplied via a single supply voltage of 2.5 V via the large bond pads indicated in Figure 5. This supplies both the digital part and the analogue part (via an internal voltage regulator) of the ASICs. The resistivity for the 2 μm thick copper layers is specified to be 0.4 Ω/cm for a 200 μm wide trace. Assuming 200 mA current consumption per chip and a uniform current density across the planes it gives a voltage drop of 75 mV to the last chip in the chain on both the V_{DD} and GND supply planes. In reality the current will not be uniformly distributed and hence the voltage drop is expected to be larger.

The ASICs are supplied by a constant current source and have two internal shunt transistors used to keep the core voltage of the chip at 2.5 V. This internal shunt requires control signals from an external regulation circuit, labelled SHUNTCTL1 and 2 in the schematic. These signals are either supplied by the on-hybrid regulator shown in Figure 6 or by an external regulator via the bond pads shown in Figure 5. The schematic of the on-hybrid regulation circuit is shown in Figure 6 and should be implemented in the area indicated in Figure 8. The voltage reference LM4121AIM5-1.2 and the operational amplifier OPA365AIDBVTG4 are both in SOT23-5 package. The passive components are all SMD 0402.

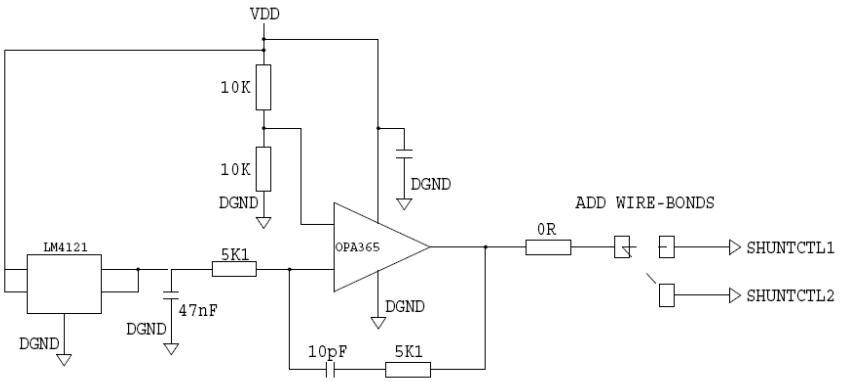

Figure 6: Shunt regulation control circuit for the serial powering scheme. The shunt control lines (SHUNTCTL1/2) are driven either from this circuit or from an external regulator via the connection pads shown in Figure 5. The area to implement this circuit is indicated in Figure 8.

4.3. High voltage bias and shield connections

The bias voltage for the silicon sensor is filtered on the hybrid and then supplied via bond wires to the bias rail and back-plane of the sensor. The bond pad locations are shown in Figure 5. The schematic of the circuit is show in Figure 7. The terminals 'HV in' and 'HV return' are the connections to the HV power supply.

The 'HV in' and 'HV out' pads and the lines between them will be at 500V potential, hence high voltage clearance is needed. No signals should be routed between the V_{DD} plane and these lines, and adequate distance should be left laterally.

The 'HV out' indicated in Figure 5 is bonded to the back-plane of the sensor. The hybrid has two bond pads to the bias rail in each corner of the hybrid as indicated in Figure 5 and Figure 8. One pad is DC connected and one is AC connected to ground. The AC connection is done via a capacitor in each corner of the hybrid close to the bond pads.

The 'HV return' has both an AC and a DC connection as indicated in Figure 7. Finally, this part of the circuit provides a connection between the HV ground and the hybrid ground and an optional connection to the shield layer via a bond wire.

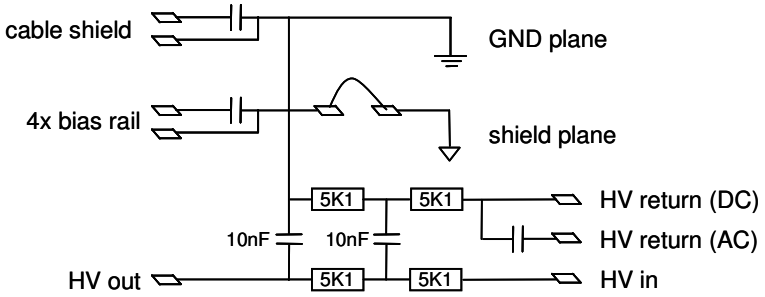

Figure 7: The schematic shows the HV filter circuit and the connection to ground and shield planes.

The 10 nF filter capacitors should be 1206 SMD components rated to 500 V. The 5.1 kΩ resistors and the AC coupling capacitor on the 'HV return' line should be 0603 SMD components. The remaining SMD components should be of size 0402.

4.4. Control and data interface

The control and data interface to the hybrid is implemented in the opposite end of the hybrid compared to the power connections. It features a row of 23 pads that can be bonded out to an interface board. Moreover there are connections to the bias rail and the cable shield as described in Figure 7. The pin assignment of the control interface is described in Table 1. Figure 8 shows the layout of the current hybrid. The circuit in the top-left corner is the control circuit for the serial powering scheme.

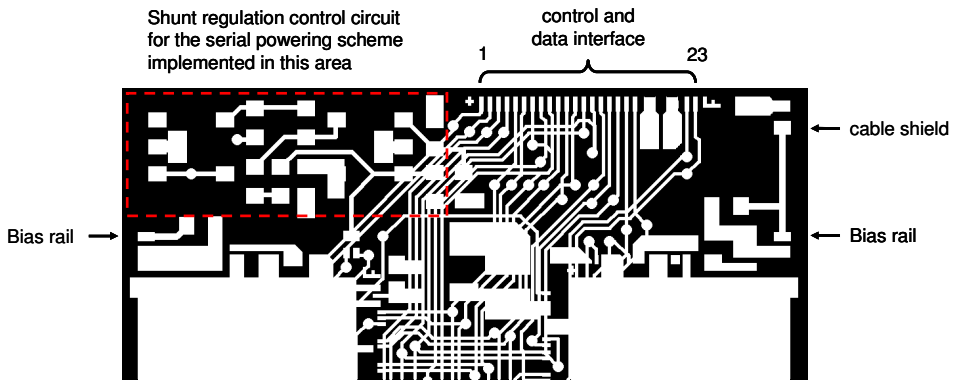

Figure 8: The Gerber screen shot shows the control interface end of the current hybrid. The 23 bond pads for control and data and the connections to the bias rail and bus cable shield are indicated.

Table 1: The table describes the 23 pads on the control and data interface.

Pad	Name	Comment
1	IDO1B	Data output (LDOB) from chip 64
2	IDO1	Data output (LDO) from chip 64
3	IDO0B	Data output (LDOB) from chip 0
4	IDO0	Data output (LDO) from chip 0
5	RESB	Connect to HardResetB on all chips
6	RES	Connect to HardResetB on all chips
7	L10B	Connect to LoneB on all chips
8	L10	Connect to Lone on all chips
9	COM0B	Connect to COM0B on all chips
10	COM0	Connect to COM0 on all chips
11	CLK0B	Connect to CLK0B on all chips
12	CLK0	Connect to CLK0 on all chips
13	BC0B	Connect to BC0B on all chips
14	BC0	Connect to BC0 on all chips
15	CLK80	Connect to ClkMode80 on all chips
16	IDO2B	Data output (LDOB) from chip 9
17	IDO2	Data output (LDO) from chip 9
18	IDO3B	Data output (LDOB) from chip 73
19	IDO3	Data output (LDO) from chip 73
20	GND	Ground
21	VDD	Digital supply
22	NTC0	Temperature sensor (NTC) connection
23	NTC1	Temperature sensor (NTC) connection

4.5. LVDS line implementation

The fast signals (40 or 80 MHz) are differential signals on the hybrid. The track width, spacing between tracks and the thickness of the BCB layer between the power plane and the signal plane (Layer 7) should be chosen to tune the differential impedance of the lines. The target value for the differential impedance of the LVDS pairs is 100 ohm for the bare hybrid and the minimum acceptable value is 70 Ω. The positive line in the pair has the bare name and the negative line has the suffix 'B'. The lines should be terminated as described in Section **Error! Reference source not found.**. The differential signals are:

LDO0(B), LDO1(B), LDO2(B), LDO3(B), RES(B), L10(B), COM(B), CLK(B) and **BC0(B)**

The differential lines should be terminated with SMD resistors in 0402 format. They should be located at the end on the differential lines close to the power end of the hybrid. The exact value of the resistances will be tuned to the effective line impedance including the ASIC inputs.

4.6. Power decoupling

The power supply plane should be decoupled at each chip with SMD capacitors. Figure 9**Error! Reference source not found.** shows the location of the decoupling capacitors on the current design. The analogue front-end should be decoupled with 100 nF in 0402 format at every ASIC as indicated by the red rectangles in Figure 9**Error! Reference source not found.**. The supply plane should be decoupled by two 100 nF and one 1 nF capacitors in 0402 format as indicated by the yellow rectangles in Figure 9. Furthermore, each pair of ASICs shares one 2.2 μF capacitor in 0603 format as indicated by the blue rectangles in Figure 9.

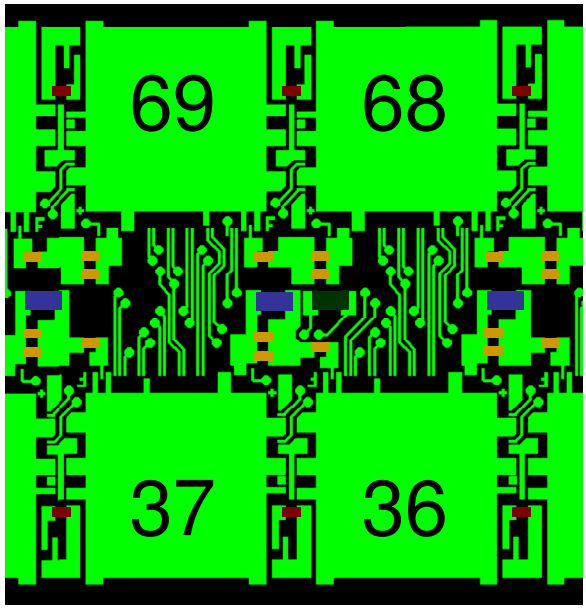

Figure 9: The figure shows the locations of the decoupling capacitors on the current kapton hybrid design. See text for details.

4.7. Temperature sensor (NTC)

The temperature of the sensor and hybrid is monitored by a Negative Temperature Coefficient (NTC) thermistor. It is implemented as a 0603 SMD component and located between the two rows of ASICs in the middle of the hybrid, indicated by the green rectangle in Figure 9**Error! Reference source not found.**. The two terminals are routed out to the control interface.

5. ASIC implementation

The footprint of the ASIC can be extracted from the supplied Gerber files and the exact location of each pad is listed in the ASIC documentation. This section specifies how the ASIC should be integrated on to the MCMD hybrid.

5.1. ASIC floor plan

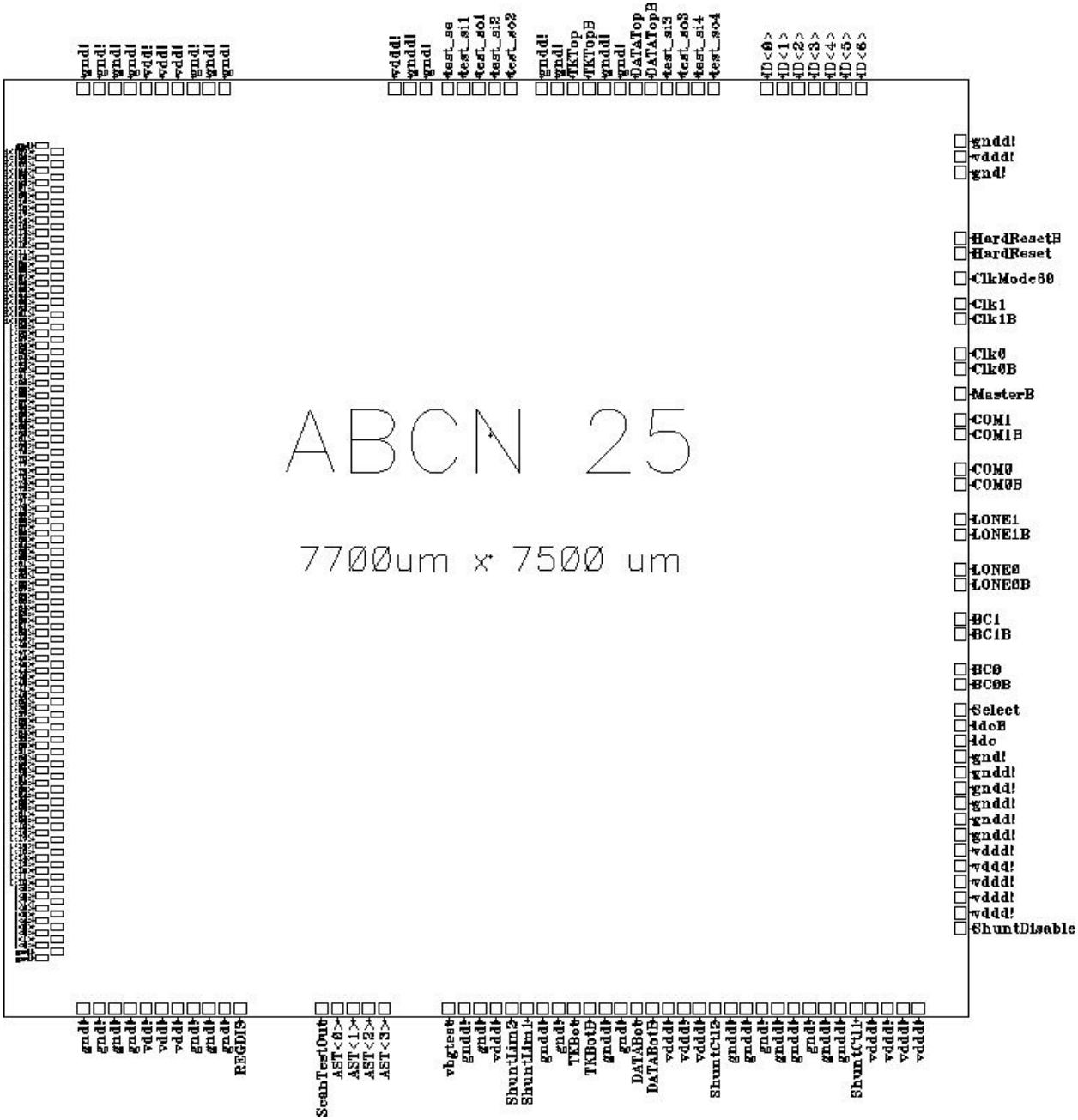

Figure 10: The figure shows the names and locations of the bond pads on the ABCN ASIC. The small pads on the left-hand side are the 128 analogue input pads plus two ground pads at the bottom end and one ground pad at the top end.

5.2. ASIC connectivity

Table 2: The table lists the required connection of all ASIC pads, omitting the 128 analogue inputs. The net names are the same as in Table 1.

Pad	Connect to	Comment
gnd!	GND	Ground connections (analogue)
gndd!	GND	Ground connection (digital)
vdd!	VDD	Digital supply voltage (2.5V)
vddd!	VDD	Digital supply voltage (2.5V)
REGDIS	GND	Disable voltage regulator for analogue voltage
ScanTestOut	N/C	Used for chip testing
AST<0-3>	N/C	Used for chip testing
vbgtest	N/C	Used for chip testing
ShuntLim1/2	VDD	Sets max shunt current in serial powering mode
TKBot(B)	N/C	Token passing, bonded directly chip to chip
DataBot(B)	N/C	Data path, bonded directly chip to chip
ShuntCtrl/2	ShuntCtl1/2	Control signal for serial powering (M-scheme)
ShuntDisable	ShuntDisable	Disable serial powering (W-scheme)
ldo(B)	LDO<0-3>	Data output from last chips in data/token chain
Select	GND	Select the primary clock & command inputs
BC0(B)	BC0(B)	Primary bunch-crossing clock input
BC1(B)	N/C	Redundancy bunch-crossing clock input
LONE0(B)	L10(B)	Primary level 0 trigger input
LONE1(B)	N/C	Redundancy level 0 trigger input
COM0(B)	COM0(B)	Primary command input
COM1(B)	N/C	Redundancy command input
Master(B)	GND	Bonded or not to select Master/Slave mode
Clk0(B)	CLK0(B)	Primary serialiser clock input
Clk1(B)	N/C	Redundancy serialiser clock input
ClkMode80	CLK80	Selects 40/80 MHz mode of serialiser
HardReset(B)	RES(B)	Hard reset signal to the chips
test_xxx	N/C	Used for chip testing
TKTop(B)	N/C	Token passing, bonded directly chip to chip
DataTop(B)	N/C	Data path, bonded directly chip to chip
ID<0-6>	GND	Chip ID bonds, internal pull-up